ADVANCED HARPSS PROCESSES FOR HIGH Q AND HIGH FREQUENCY INERTIAL SENSORS

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Anosh Daruwalla

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ADVANCED HARPSS PROCESSES FOR HIGH Q AND HIGH FREQUENCY INERTIAL SENSORS

Approved by:

Dr. Farrokh Ayazi, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Hua Wang
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Azadeh Ansari
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Peter Hesketh
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Oliver Brand
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: August 20, 2019

To the loving memory of Manda Gokhale and Rustom Daruwalla

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LIST OF SYMBOLS AND ABBREVIATIONS

6DOF	6 Degree-Of-Freedom
A	Electrode Area
ADEV	Allan Deviation
A_g	Angular Gain
AlN	Aluminium Nitride
A_n	Amplitude of P-wave
Ar	Argon
ARW	Angular Random Walk
B	Boron
BAW	Bulk Acoustic Wave
BCl_3	Boron Trichloride
BDLR	Beam Distributed Lame Mode Resonator
B_n	Amplitude of SV-wave
BOX	Buried Oxide
C_4F_8	Octafluorocyclobutane
$c_{i,j}$	Elastic Constants of Silicon
Cl_2	Chlorine
CMOS	Complementary Metal-Oxide Semiconductor
d	Gap Size
DRIE	Deep Reactive Ion Etching
ENEA	Electrical Noise Equivalent Acceleration
Epipoly	Epitaxially-grown Polycrystalline Silicon

Eu	Deformation Potential
f_0	resonance frequency of gyroscope
FDLR	Frame Distributed Lame Mode Resonator
fQ	Frequency x Quality factor
G	Gibb's free energy
g_0	Capacitive HARPSS gap
GPS	Global Positioning Systems
HARPSS	High Aspect Ratio combined Poly and Single-crystal Silicon
HF	Hydrofluoric Acid
HF2LI	High Frequency, 2 inputs
IMU	Inertial Measurement Units
IoT	Internet Of Things
IP	In-Plane
K_B	Boltzmann's constant
K_{BAW}	Mechanical Spring Constant
K_E	Electrostatic Spring Constant
KOH	Potassium Hydroxide
LE	Length Extensional
LF	Low Frequency
LPCVD	Low Pressure Chemical Vapor Deposition
M	Effective Mass
MEMS	Micro Electro Mechanical Systems
MNEA	Mechanical Noise Equivalent Acceleration
Mo	Molybdenum
O_2	Oxygen

OOP	Out-Of-Plane
PCB	Printed Circuit Board
PECVD	Plasma Enhanced Chemical Vapor Deposition
PML	Perfectly Matched Layer
pSOI	Polysilicon On Insulator
Q	Quality factor of the resonator
q_1	Drive amplitude of gyroscope
R_m	Motional Impedance of resonator
SCS	Single Crystal Silicon
SEM	Scanning Electron Microscope
SF	Scale Factor
SF_6	Sulphur Hexafluoride
SFD	Squeeze Film Damping
$S_{i,j}$	Strain
SOI	Silicon On Insulator
SV	Secondary Vertical
t	Resonator Thickness
TCF	Temperature Coefficient of Frequency
TED	Thermoelastic Damping
TEOS	Tetraethyl orthosilicate
TIA	Transimpedance Amplifier
TMAH	Tetramethylammonium hydroxide
TNEA	Total Noise Equivalent Acceleration
TSV	Through Silicon Via
VHF	Very High Frequency

Vp	Polarization Voltage
Vq	Quadrature Voltage
Vt	Tuning Voltage
W	width of resonator
WLP	Wafer Level Packaged
ZRO	Zero Rate Output
γ	Wave Number
ΔQ	Quality factor split
ε_0	Permittivity of Free Space
θ	Angle of reflection
ρ	density of silicon
ω_0	Angular Frequency

SUMMARY

The surging growth of the Internet of Things (IoT) is driving demand for microelectromechanical systems (MEMS) devices in areas such as navigation and tracking systems, smart grids, 5G and building automation. One of the main reasons for this, is that IoT can leverage several core functions and benefits of MEMS, wherein these devices can effectively meet the requirements of many IoT applications, such as low power consumption, small form factor and cost effectiveness, to name a few.

The objective of this thesis is to introduce several advances into the HARPSS fabrication platform to improve the performance metrics of such resonant MEMS devices and enable new functionalities. For this purpose, we first delve into the evolution of the HARPSS process, and the advancements that have taken place over the years. The addition of newer features in the process over the years has helped enable high performance MEMS devices, to meet the growing requirements of emerging IoT technology.

Many resonators including bulk acoustic wave (BAW) gyroscopes require ultra-high quality factor (Q) in the order of 1M to improve signal to noise ratio. The use of isotropic device layers such as thick epitaxially-grown polycrystalline silicon (epipoly) can enable Akhiezer-limited Qs due to suppressed thermoelastic damping (TED) and anchor loss in centrally-supported gyroscopic disk resonators. However, thick epipoly is prone to large residual stress at high processing temperatures (>900°C). Hence, a reduced-temperature HARPSS process has been devised and prototype thick solid-disk epipoly BAW gyroscopes have been fabricated on a 45um pSOI wafer and tested in a preliminary effort, yielding large Qs of 1M, in the first part of the thesis. These gyroscopes were mode

matched to yield an ARW of 0.01deg/rthr, with a scale factor as large as 7nA/dps, which can be used in IoT applications such as smart cars and wearable health monitoring, where detection of small movements is of prime importance.

Another important performance metric of a silicon resonator is the temperature stability at high frequencies. Hence, the second part of this thesis involves research on a novel design of wafer-level-packaged (WLP) high-Q capacitive Distributed Lame Mode resonators (DLR), which enable significant improvement in their figure of merit, extending their frequency into the VHF range while keeping their motional resistance low. The nano-gap distributed Lamé mode resonators (DLR) show high Qs of 250k at VHF frequencies >50MHz with low motional impedances of <1kΩ, which cannot be attained by conventional square Lame modes at those frequencies, combined with a high temperature-frequency turnover point of greater than 90°C, making them suitable candidates for low-power temperature-stable timing applications at VHF and possibly even UHF range, 5G applications.

Lastly, the multi-transduction capability of capacitive resonators can be combined using piezoelectric transduction, and by scaling the capacitive gaps to sub-100nm, high performance BAW sensors can be enabled. In the third part of this thesis, a frequency-output piezoelectrically-transduced resonant BAW accelerometer is introduced, combining a sub-100nm gap HARPSS process with a metal-less high-frequency AlN-on-silicon resonator, with a quality factor of 3800 in air. The 360kHz high-bandwidth device operates based on electrostatic softening effect and utilizes a novel moving electrode design to extend the dynamic range of the accelerometer, with a scale factor of 0.91Hz/g. Such high BW accelerometers can be used in IoT health monitoring applications.

CHAPTER 1. INTRODUCTION

1.1 Integrated Inertial Sensors for Navigation

Navigation is an integral part of the military and automobile industry. Inertial navigation works on Einstein's theory of relativity where different parameters such as position, orientation and velocity of a moving object are calculated, using the aid of accelerometers (motion sensors) and gyroscopes (rotation sensors). The earliest navigation systems were used pioneered Robert Goddard and used by Germany in World War 2, to adjust the azimuth of a rocket in flight. The first automobile navigation system called the Electro Gyro-Cater was commercialized by Honda in 1981 and used a gas gyroscope to detect both rotation and movement as shown in Figure 1[1]. These were few of the first sensors to be used for navigation purposes. In the coming years, the global positioning system (GPS) as it came to be called, allowed users to determine their location and velocity at any time of the day in all weather conditions on a global level. This is done using an array of about 30 satellites for people with receivers in their phone or car to pinpoint their location anywhere on earth, with an accuracy of a few meters.

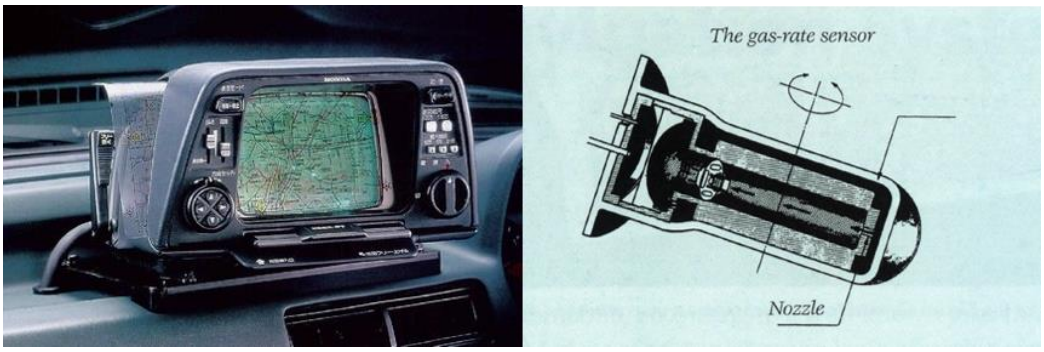

Figure 1 – The Honda Electro Gyro-Cater (left) and a cross section of the helium gas gyroscope used for inertial navigation [1].

Today, GPS is a multi-use, space-based radio navigation system owned by the US Government and operated by the United States Air Force to meet national defence, homeland security, civil, commercial, and scientific needs. GPS currently provides two levels of service: Standard Positioning Service (SPS) which uses the coarse acquisition (C/A) code on the L1 frequency, and Precise Positioning Service (PPS) which uses the P(Y) code on both the L1 and L2 frequencies. Access to the PPS is restricted to US Armed Forces, US Federal agencies, and selected allied armed forces and governments. The SPS is available to all users on a continuous, worldwide basis, free of any direct user charges. The specific capabilities provided by SPS are published in the Global Positioning System Performance Standards and Specifications [2].

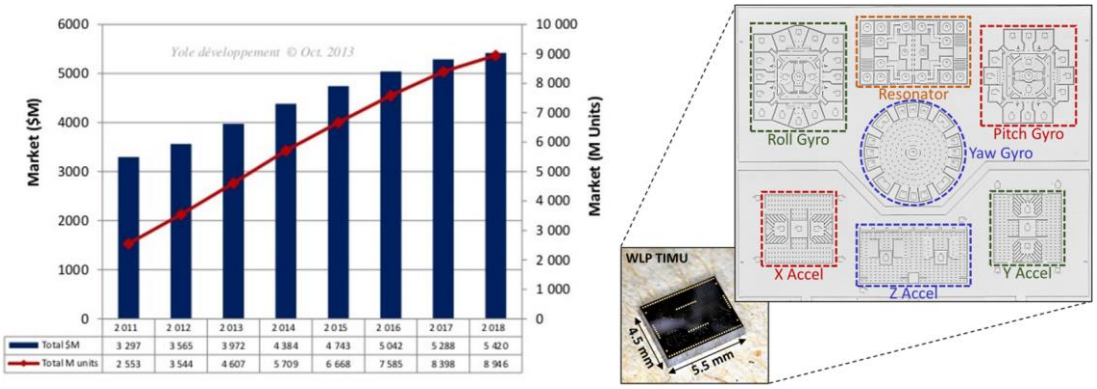

Figure 2 – The forecast of market revenue for inertial MEMS as predicted by Yole Development in 2013 (left) [3], and a wafer level packaged 4.5mm x 5.5mm 6-degree-of-freedom high Q inertial sensor die (right) [4].

Inertial Navigation Sensors based on Inertial Measurement Units (IMU) are units of devices that are primarily used in the navigation systems to accurately measure the motion of an object in space, for military and commercial navigation purposes. Until recently the weight and size of inertial sensors has prohibited their use in domains such as personal navigation. Recent improvements in the performance of small and lightweight

micromachined electromechanical systems (MEMS) inertial sensors have made the application of inertial techniques to such problems possible. This has resulted in an increased interest in the topic of inertial navigation, however current introductions to the subject fail to sufficiently describe the error characteristics of inertial systems. The most common IMU devices include the accelerometer, for linear motion sensing and the gyroscope, which is used for rotational motion sensing. Needless to say, the rise of navigation system technology over the past decade has led to the need for IMU that are more robust, durable and can sense signals with a large accuracy. This would mean that these devices should have the ability to sense very small signals. Also, as the IMU are usually placed in a small area on the motherboard of a phone or the navigation unit of a car, they need to be extremely tiny in size, in the order of microns. Hence, the use of MEMS for IMU becomes imperative. MEMS allow for the fabrication of IMU using common substrates such as silicon and germanium and may be capacitive, piezo-electric or magnetically transduced at a low cost. In Figure 2, data taken by Yole Development shows that there is a significant increase of MEMS for IMU products and the market revenue is expected to be $5.5B by 2018 with 9000 units sold [3].

1.2 High Performance of Inertial Sensors

To facilitate high performance inertial sensors for integrated IMUs, various approaches have been used. One approach for enhanced capacitive sensing and actuation is to reduce the gap size to deep-sub-micrometer and nanometer scales. For capacitive devices, the smaller the gap size, the higher the sense capacitance and hence the device sensitivity. For gyroscopes, the High-Aspect-Ratio-combined-Polysilicon-to-Single-crystal-Silicon (HARPSS) process [5]–[12] has previously shown that while reducing the

gap size to sub-micron level, the device performance is enhanced greatly. Another way of improving device performance is to increase the size and hence the mass of the device. However, for MEMS applications, a small size in the order of hundreds of microns is generally preferred. As shown in Figure 1, a 6-degree-of-freedom inertial sensor die designed at Georgia Tech [4] can be as small as 4.5mm x 5.5mm in dimension, which would have the capability to easily fit inside a consumer-used device such as a mobile phone. The capacitively actuated and sensed devices in this inertial sensor die had sub-micron gaps and were fabricated using the HARPSS process.

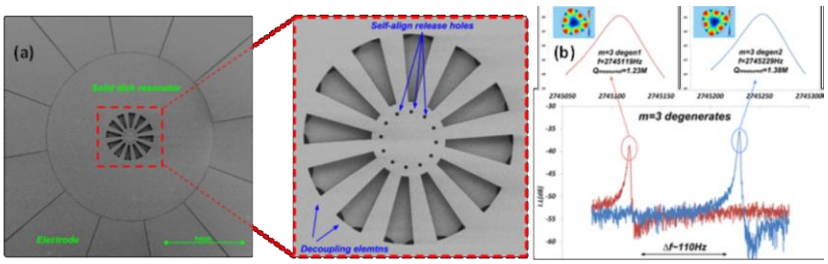

Figure 3 - (a) SEM view of a substrate-decoupled BAW gyroscope which shows (b) very high-quality factors and large frequency splits [13].

The *Q* of a MEMS gyroscope is an important parameter which affects the noise and hence the performance. For mode matched gyroscopes, the scale factor of the device is boosted by mechanical *Q* amplification, which in turn improves the signal-to-noise ratio. Also, for mode matched operation in pitch and roll gyroscopes, we need out-of-plane electrodes as well as slanted electrodes to effectively cancel quadrature. All these features can be enabled by the HARPSS process in silicon, as it currently stands, as explained in chapter 2. Hence, to attain low noise levels, it is imperative that devices need to be designed to get high quality factors, in the range of 500k to over 1 million [13]. This is however, not easy to achieve with current technology, since disk gyroscopes suffer from large anchor

losses due to the anisotropy of silicon. As shown in the Figure 3, decoupling notches can be introduced, but these add thermoelastic damping to the device thereby reducing its *Q*. Hence, we need to migrate the HARPSS process on isotropic substrates like epitaxially grown polysilicon. The details of this process are explained in chapter 3.

1.3 High Frequency Silicon Resonators

Other than having gyroscopic applications, silicon MEMS resonators have drawn a great amount of attention for timing applications during the past two decades due to their small size, low cost, and integration compatibility. However, these elements still have not been able to replace their quartz counterpart in many applications. The bottleneck for silicon MEMS resonators is the lack of temperature stability at high resonance frequency. Currently, the major manufacturers of temperature stable MEMS oscillators are SiTime, Silicon Labs, Murata, to name a few. These companies specialize in silicon resonators, which act as timing elements, and are temperature compensated using various techniques. This type of temperature stability in a silicon timing element is usually achieved by ovenizing a highly-doped square Lamé mode resonator with a quadratic TCF profile at its turnover point with a resonance frequency typically below 10MHz [14]. Square Lamé mode resonators have been popularly used to attain high *f.Q* products owing to their ability to produce *Q*s over a million with frequencies in the range of 10s of MHz [15], [16]. Figure 4 shows one such resonator at a frequency of 77MHz [17]. Furthermore, the relatively low frequency of square Lamé mode resonators requires the use of up-converting frequency synthesizers to get to higher frequency oscillators, leading to additional phase noise and larger power consumption.

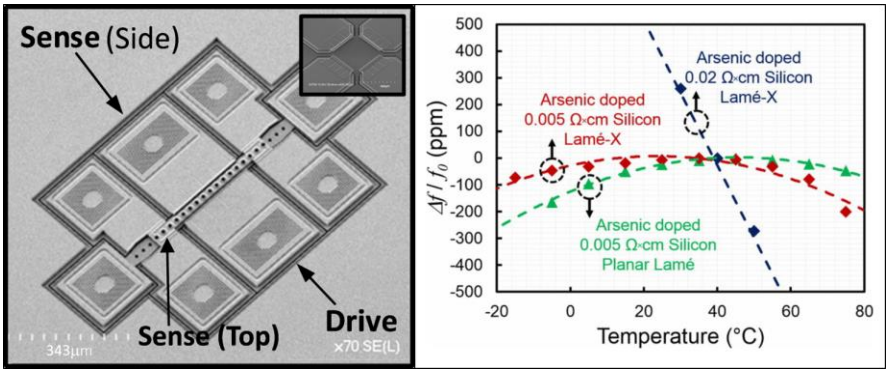

Figure 4 – High frequency Lame mode at 77MHz with a turnover point at 40°C, which is a good candidate for high frequency MEMS timing applications [17].

1.4 Internet of Things and MEMS

While navigation has been one of the main markets for MEMS technology, the IoT has caused many new emerging applications and desire for higher performance MEMS. The most important parameter about MEMS devices, is that they often behave similarly to their larger counterparts with some notable differences. One of the key differentiators being, that the sheer number of MEMS devices that can fit into a larger device like a smartphone. A range of sensors like the ones mentioned previously, and other MEMS devices can be packed into a pocket-sized smartphone. MEMS are also significantly cheaper than their larger counterparts due to their manufacturing process. MEMS are micro-machined, and made with many of the same techniques used to make integrated circuits and semiconductors. The process compatibility allows manufacturers to produce MEMS in batches without much need for new equipment at many semiconductor manufacturers.

The internet of things can leverage many benefits of MEMS devices. These include low power consumption, small form factor and cost effectiveness [18]. The reduction in power extends the lifespan of any device. MEMS devices usually face the same power

requirements as their larger counterparts. MEMS can also be easily added to heavy machinery like a car or phone, because of their small size. This makes them extremely unobtrusive by nature. The cost effectiveness of MEMS devices comes from the fact that they use easy and cost effective techniques during mass production. Figure 5 below shows a map of the IoT applications and its key technologies [19].

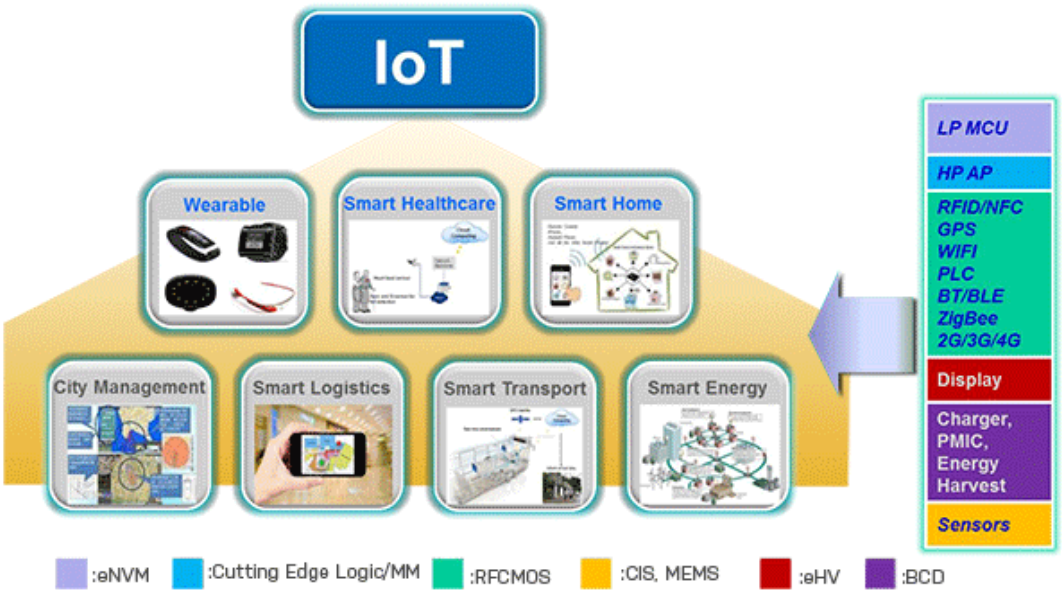

Figure 5 – Internet of Things Applications and Key Technologies, with MEMS sensors being an important block of its structure [19].

While the IoT uses a vast array of sensors such as microphones, pressure sensors, gas sensors, biosensors, magnetometers, etc. the focus of this thesis is primarily IMU which consists of gyroscopes, accelerometers and timing resonators, which are used for navigation and sensing applications. In order to achieve high performance of these devices, we use the HARPSS process to fabricate them. This process enables sub-micron gaps in the order of 90-350nm, which is the range of values that the devices in this thesis are designed for. However, in order to design these high performance MEMS sensors and to

facilitate further advancements in the HARPSS process, it is first important to study this process in detail and to highlight the changes that it has gone through since it was first conceived in the year 2000 [6]. Once we have drawn out the evolution of this process, the further chapter 3 to 5 will highlight the advanced steps in the HARPSS process and also compatibility with isotropic epipoly substrates as well as piezoelectric films such as AlN. Using these additional features in the process, high performance devices such as epipoly disk gyroscopes for smart cars, high frequency timing resonators for 5G applications and high bandwidth BAW accelerometers for health monitoring are designed and fabricated, which form the bulk of this research.

CHAPTER 2. HARPSS PROCESS FOR NANO-GAP BULK ACOUSTIC WAVE INERTIAL SENSORS

The abbreviation ‘HARPSS’ stands for High-Aspect-Ratio-combined-Poly-and-Single-crystal-Silicon process. To facilitate advanced features using the HARPSS process, it is essential to study and review the previous versions of the process. These versions will be used as the basis for the fabrication of high-performance devices, with enhanced features that will enable certain characteristics such as higher quality factors, higher operating frequency with turnover points, and lastly the combining metal-free piezoelectric stacks to silicon. Prior work shows that to reach Akhiezer limited *Q*s using single crystal silicon (SCS), various resonator structures have been designed, most common being wineglass modes in disk resonators and Lame modes in square resonators. Lame modes are better suited to get high *Q* resonators; this has been demonstrated in many designs with the resonator tethered at the nodes. While such resonators provide the high *Q*s used in various timing applications, the frequency of these resonators is limited by fabrication constraints, as the frequency goes higher. It is important to study these processes because it is the basis for advanced versions of HARPSS which would go on to address some limitations of the existing processes.

2.1 Various Renditions of the HARPSS Process

The HARPSS process which has been used over the last two decades, has been well documented and has many variations, all of which are listed in table 1. For the brevity of this document, only the literature consisting of process variations or enhancements to their

previous versions have been included. The first HARPSS process [5]–[7] consisted of LPCVD polysilicon devices which were formed by filling trenches inside a regular silicon wafer, which were released by etching away the silicon and shielding the polysilicon. Due to the nature of polysilicon deposition in trenches, this process could only enable vertically thin structures. One of the other reasons for such a design was the fact that the Bosch DRIE process was fairly new at that time and was not well characterized for larger yield. While these devices yielded novel gyroscope designs, emerging technologies demanded for more robust MEMS devices with higher performance. Hence, a change had to be made in the process, where devices needed to be formed in silicon itself for more rigid, high frequency wider structures. The process therefore, had to be then migrated to an SOI wafer [20], which would enable release via the buried oxide layer. With the advent of SOI wafers, it enabled MEMS devices to be more BAW oriented and rigid structures, which could be released easily and thereby used in applications requiring durable and high performance of devices.

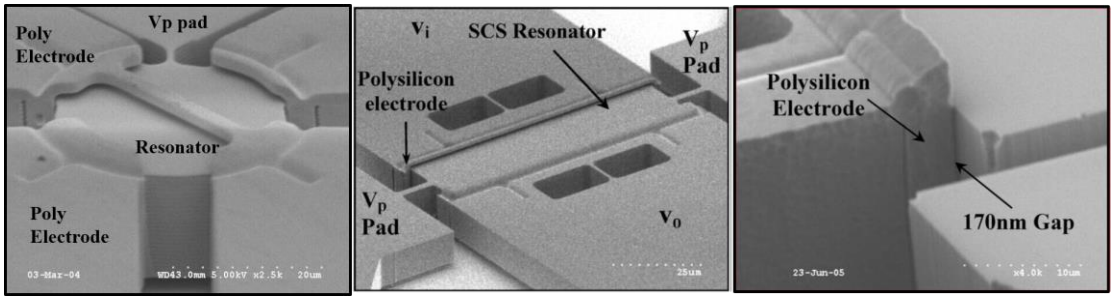

Figure 6 – Side supported disk (left), SiBAR (middle) and a close up of the HARPSS nano-gap (right) in some early fabricated HARPSS devices [21].

Figure 6 shows some early devices fabricated using this type of HARPSS process, with the nano-gap [21]. These versions of the process were short 3-mask processes that could enable capacitive transduction of in-plane modes. This process involved the following

steps. First, trenches were etched into a 20-40um device layer on an SOI wafer, using an oxide mask. Next, a thin-film oxidation was done to form the capacitive nano-gap, which was in the range of 250-400nm at 1100°C. After this, LPCVD in-situ doped polysilicon was deposited at 588°C and was etched back to the surface. Then the oxide mask at the surface was patterned to form the connections for the electrodes. The next step was to once again deposit LPCVD polysilicon with the same conditions as earlier to connect the device layer to the poly inside the trenches. Next, using the third mask, the polysilicon was etched from the trenches where it wasn't needed and the HARPSS electrodes were formed. Finally, the devices could be released in HF. This process allowed high frequency, stiffer devices to be fabricated which could be released by HF, which was not possible earlier. Another advantage was that since the devices were made out of silicon itself, as compared to polysilicon earlier, they were much more robust and durable, and also had minimum fabrication imperfections, such as voids formed because of polysilicon deposition. While this process had a few drawbacks, it was an important version of the HARPSS process on which all the processes to follow have been based. It was also easy to fabricate except for the etching of the polysilicon from trenches, all the other steps were fairly well characterized in clean rooms.

There have been further renditions to the process in terms of using oxide islands within the device [22], self-polarized devices by addition of nitride annealing [23], using the <111> substrate SOI [24], self-alignment between masks to reduce fabrication effects [25], and also incorporating joule heating and post fabrication metal depositions [26]. The use of oxide islands in the device was important to change the temperature characteristics of the inherent silicon device by addition of oxide. This reduced the frequency drift of a silicon

resonator with respect to temperature, to allow these devices to be temperature-stable across commercial temperature ranges (-40°C to 85°C). Addition of annealing to the sidewalls was another addition to the above 3-mask process. This allowed the undulation or scalloping of trenches caused by Bosch DRIE to smoothen out considerably, thereby enabling smaller gap sizes for capacitively transduced devices. This annealing is an extremely important step in the process, and is done even in the latest process that is used today, which is a lot more complex than the one described above.

While the above 3-mask HARPSS process proved to be extremely ground-breaking in being able to enable robust BAW resonators, its main drawback was the fact that only in-plane vibrating devices could be fabricated. While this was useful in fabricating prototypes of various devices with reasonable performance, improving technology such as 6DOF applications, it was essential to add out-of-plane features. While it was natural to use similar thin sacrificial oxides and polysilicon electrodes for OOP operations, incorporating them in the current process flow was a challenge. This was because, the trenches were vacant at the time of oxide formation for the OOP electrodes, and had to be once again filled with some material so that the formation of the OOP electrodes can be fabricated.

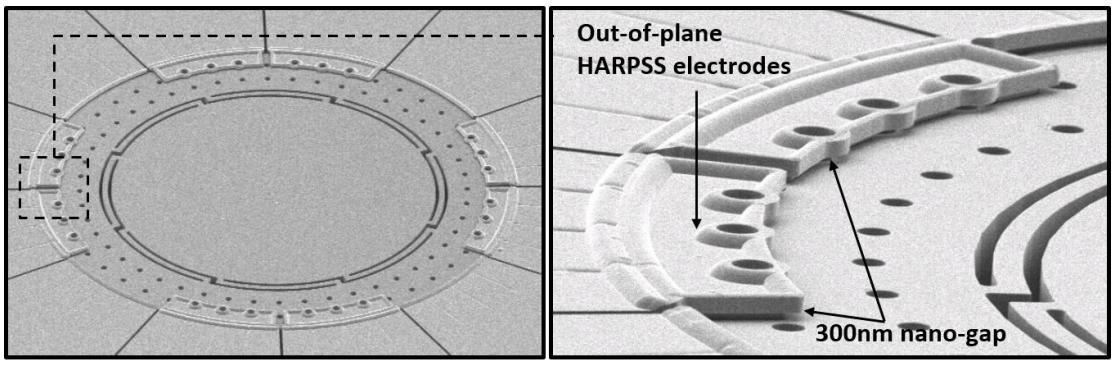

Figure 7 – Pitch and roll BAW annulus using out-of-plane HARPSS electrodes (left), and a close up view of the 300nm OOP gap (right) [12].

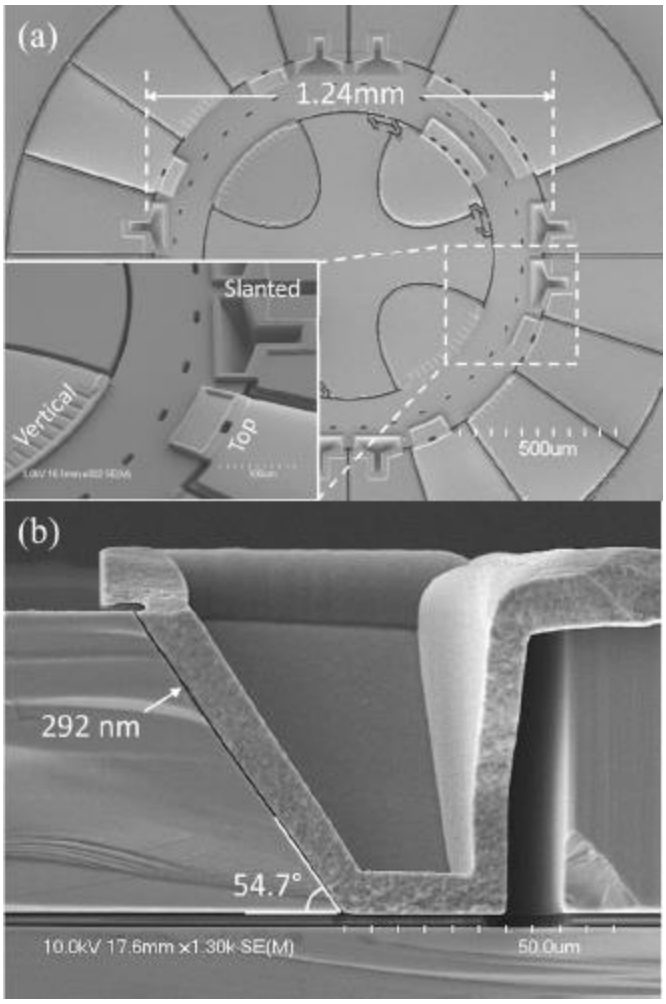

Figure 8 – SEMs of fabricated XY gyroscope showing (a) Top view with diameter of the annulus which is 1.24mm. Inset shows zoom-in view of the three types of electrodes. (b) Cross-sectional view of the slanted electrode with a slanting angle of 54.7° and a gap-size of 292nm. These features were added using slanted sidewalls in the HARPSS process [4].

Hence, it was decided that additional TEOS depositions needed to be added to the process, to cover up trenches during the LPCVD polysilicon deposition for the top electrodes. This made the process much harder because refilling trenches by TEOS was not a straightforward step. TEOS based oxide is high stress in nature, and several steps of thin deposition and annealing had to be carried out to prevent the film from cracking and propagating the cracks to the entire wafer. Figure 7 illustrates an annulus fabricated using

out-of-plane electrodes [12]. This process which used 5 masks, allowed us to fabricate devices with OOP operation such as pitch and roll gyroscopes, and also OOP accelerometers. The use of this process enabled inertial sensor operation in all 6 axes, or 6DOF operation, which was coherent with the emerging trends of MEMS inertial measurement units. Enabling both in-plane and OOP features also allowed us to use gyroscopes in a fully mode-matched operation. Doing this resulted in improvement of performance for inertial measurement units, especially those in the OOP direction.

While it was seen that the above process flow resulted in features that could enable mode-matching of gyroscopes, they still suffered from large quadrature, which was caused by the degenerate modes not being fully decoupled. This in turn affected the noise performance of the device. To mitigate this issue, slanted sidewalls had to be further incorporated with the process [27]. The devices shown in the TIMU die in Figure 2 of chapter 1 and a further zoomed in image of the same device in Figure 8, are fabricated using the addition of slanted sidewalls, which is the most recent version of the HARPSS process. This process added a wet-etching step of using KOH (or TMAH) to etch 54° angled electrodes in the device. Addition of this step made the process further challenging, however the resulting devices had much higher performance which were not limited by quadrature in the gyroscopes. Figure 9 shows the complete HARPSS process, as it stands today. The Table 1 below shows a listing of HARPSS process variations for new features being added to the process.

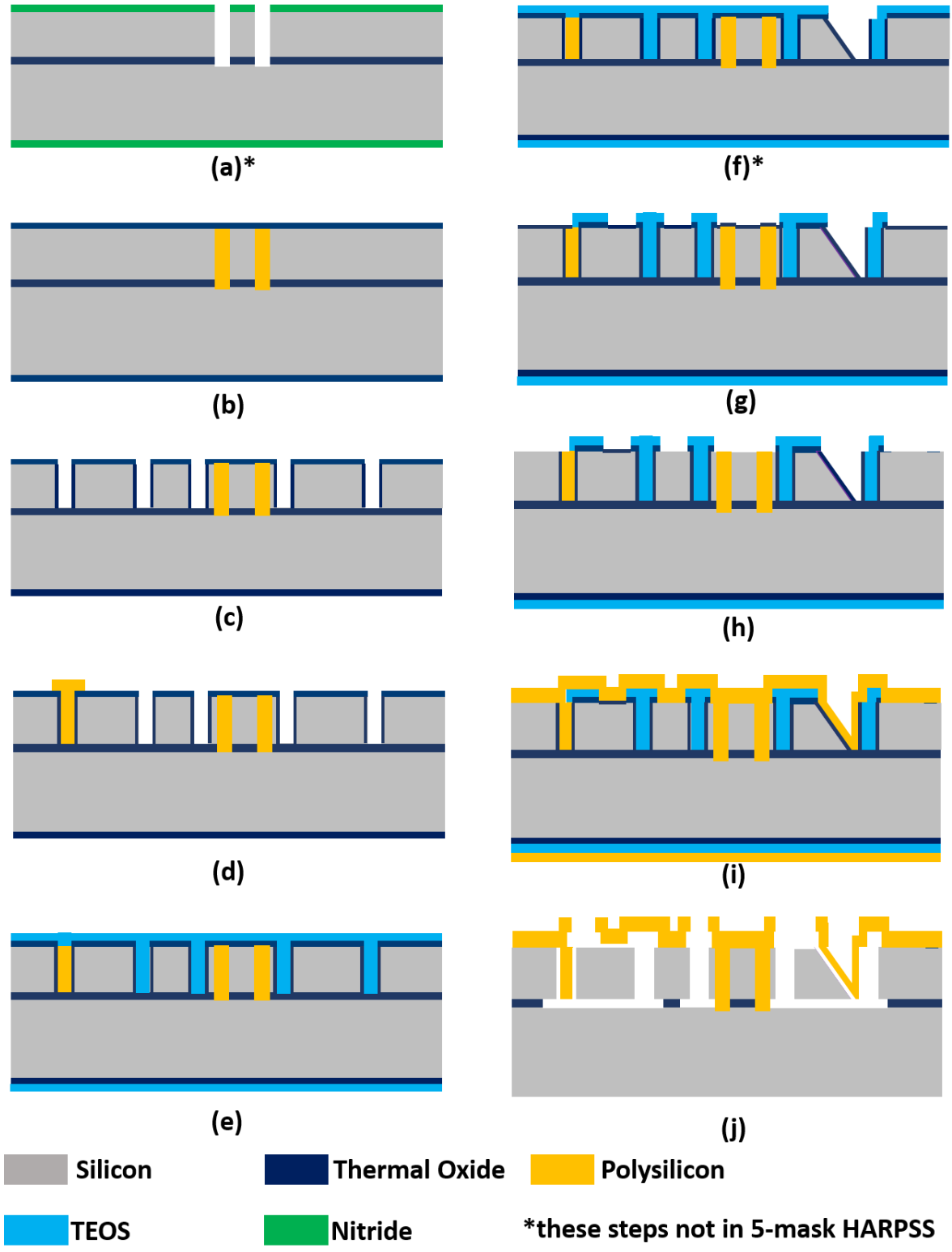

Figure 9 – Current HARPSS process flow, enabling IP, OOP and slanted electrodes.

Table 1 : Chronological listing of enhancements in HARPSS processes.

Paper	Notable features	Electrode Capability
Ayazi, et al, 2000 [5]	Original process	In-plane
Pourkamali, et al 2003 [20]	Use of SOI wafer	In-plane
Pourkamali, et al, 2004 [21]	3-mask process	In-plane
Abdolvand, et al, 2004 [22]	Oxide islands	In-plane
Pourkamali, et al, 2004 [28]	Reduced motional impedance	In-plane
Zaman, et al 2004 [29]	High Q	In-plane
Pourkamali, et al 2005 [30]	First HARPSS SiBAR	In-plane
Johari, et al, 2007 [24]	<111> substrate	In-plane
Pourkamali, et al 2007 [31]	Device encapsulation	In-plane
Rais-Zadeh, et al, 2008 [25]	Self-aligned process	In-plane
Johari, et al, 2008 [10]	OOP large gap	In & out of plane
Samarao, et al, 2009 [26]	Post fabrication metal deposition	In-plane
Samarao, et al, 2010 [23]	N_2 annealing on sidewalls	In-plane
Samarao, et al, 2011 [32]	Piezo-stack addition	In-plane
Sung, et al, 2011 [12]	OOP HARPSS gap addition	In & out of plane
Wen, et al, 2017 [27]	OOP Slanted electrode addition	In, out and OOP slanted

2.2 High Q Disk Resonators with Gyroscopic Modes

Since one of the objectives of this research is to use the HARPSS process for high quality factor gyroscope applications, it is also beneficial to study the disk resonators fabricated in literature for this purpose. Disk resonators in SCS are excellent candidates to achieve high quality factors in the range of a million, and both the N=2 and N=3 wineglass modes have been published, showing large *Q*s. The main mechanism for energy dissipation in wineglass modes is the support, and designs containing center and side supported tethers have been developed. Anchor loss, also known as support loss, is the radiation of energy from the device to the surroundings through vibration of the supporting structure [33]. It is difficult to express a closed-form expression of anchor loss, as the wave that irradiates from the device may reflect on boundaries, cracks or defects and interfere either constructively or destructively with the standing wave inside of the resonator [34]. To compute an estimated value of support loss, it is usually assumed that the surrounding is defect-free, infinite and can be implemented computationally by using a perfectly matched layer (PML) [35]. Under these assumptions, the anchor loss can be computed efficiently in COMSOL.

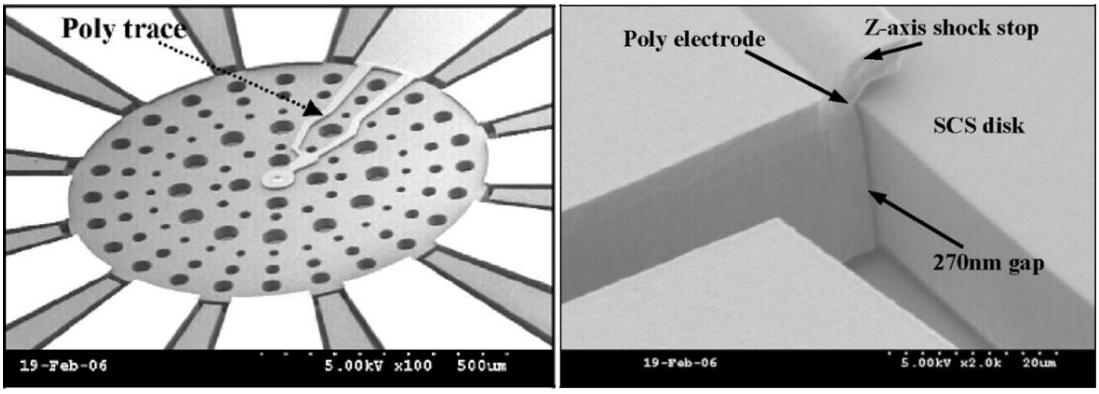

Figure 10 – Center supported N=3 disk using HARPSS process showing the poly trace for polarization voltage (left) with a 270nm gap using a polysilicon electrode (right) [8].

For mode matched gyroscopic modes, one cannot use the N=2 mode in SCS because of non-degeneracy of the mode due to the anisotropic nature of the material. Hence, we must design disks using N=3 degenerates, with high *Q*s, for mode matched gyroscopic applications. The simplest support mechanism to reduce dissipation in disks include center supported disks with notches [13] to improve support *Q* and spring decoupling structures [9], [11], [36], [37]. However, this introduces TED to the disk which reduces *Q* via this mechanism. There has also been one instance of using side supports for the n=3 mode with a high *Q* [38], however, doing so reduces the number of electrodes around the disk which might be used for quadrature cancellation for the gyroscope design. Disk using diamond instead of silicon has also been designed, since diamond has a larger Akheizer limit as compared to silicon [39], however only radial mode has been measured, and there have also been attempts at high *Q* using glass substrates [40] in the OOP mode, both which cannot be used for mode-matched gyroscopes. Table 2 lists the various mode shapes in literature, divided by side and center supports. One such gyro showing a center supported disk is shown in Figure 10.

Table 2: Wineglass mode resonators in silicon differentiated by support location.

Paper	Support location	Resonator mode	Q	Frequency (MHz)	Device material
Abdelmoneum, et al, 2003 [41]	Side	N=2	98,000	73	Silicon
Pourkamali, et al, 2004 [42]	Side	N=2	39,000	147	Silicon
Lee, et al, 2008 [43]	Side	N=2	2M	5.4	Silicon
Zarifi, et al, 2016 [44]	Side	N=2	12000	2.8	Silicon

Xou, et al, 2017 [38]	Side	N=3	1.5M	0.9	Silicon
Johari, et al, 2006 [8]	Center	N=3	243,000	6	Silicon
Johari, et al, 2008 [10]	Center	N=3	125,000	5.83	Silicon
Mirjalili, et al, 2015 [13]	Center	N=3	1.3M	2.7	Silicon
Serrano, et al, 2015 [9]	Center	N=3	68,000	4.3	Silicon
C. H. Ahn, et al, 2015 [37]	Center	N=2	101,000	.25	Silicon
Rahafrooz, et al, 2017 [36]	Center	N=3	92,000	7	Silicon

From the table, it is clearly seen that the quality factors in the center supported disks are higher than the side supported ones, and also for N=3 modes as compared to N=2 modes. Hence, to design a high-performance gyroscope, it is imperative that this must be taken into account. Furthermore, while these entries in the table have fairly large quality factors, it is worth investigating if *Q*s close to the Akhiezer limit can be achieved. The (1 for the mechanical noise of a gyroscope is given by:

$$\Omega_{\min} = \frac{1}{2\lambda q_1}\sqrt{\frac{4k_B T_0}{\omega_0 M Q}} \tag{1}$$

where q_1 is the drive amplitude, k_B is the Boltzmann constant, T is the temperature, ω is the angular frequency, M is the effective mass and Q is the quality factor of the device. This equation shows that by increasing the quality factor by a factor of 10, it is possible to further reduce the noise. Also, having a larger Q increases corresponding drive amplitude q_1 and a large disk may be designed for larger M. In order to achieve these large quality factors, the usage of a solid disk (without release perforations) becomes important, hence releasing them via back side holes have to be added to the process. One of the other problems that SCS encounters while designing gyroscopes, is the asymmetry of the n=3 mode shape

(explained in detail in chapter 3). For this purpose, we must consider more isotropic materials such as epitaxially grown polysilicon substrates to fabricate such devices. Because of this, the standard HARPSS processes that were used earlier need to be modified greatly to accommodate the change in substrate. One of the key aspects of this research is to incorporate these changes in the current process which enables other substrates such as polysilicon achieve ultra-high mode-matched quality factors. Chapter 3 explains in detail the addition and modification of various steps to the process and also addresses the challenges faced in doing so.

2.3 Lame Mode Resonator Timing Elements

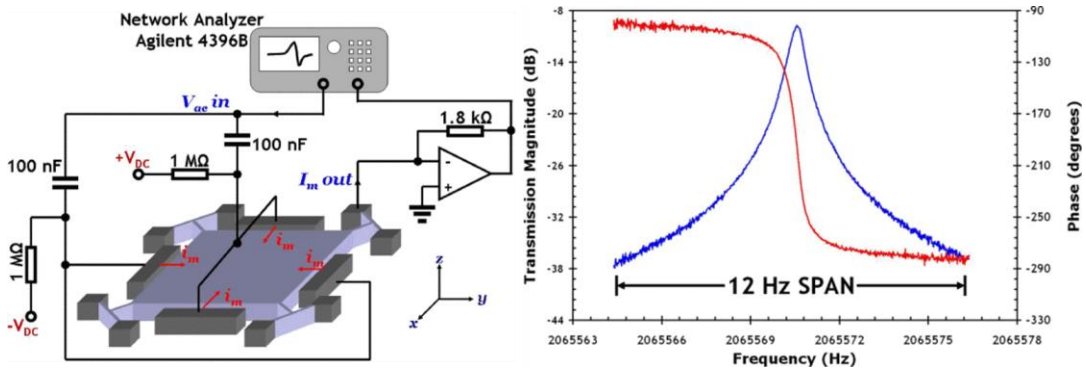

Figure 11 – Setup of a high Q square Lame mode (left), and the measured quality factor (right) [16].

The Lame mode is known to be the most widely used mode shape for resonator timing applications owing to its ability to show a turnover point at the temperature coefficient of frequency (TCF). At the turnover point, the frequency of the device is constant at that temperature, and therefore if the resonator can be held at the same temperature over its operation, we can design extremely temperature stable oscillators using that mode shape. Various types of tethers have been designed to get high *Q*s for these devices such as T

shaped tether structures [16], [45], and tether-less cross-sectional mode shapes [17], both of which are shown to increase *Q* as compared to conventional rectangular tethers. However, most of these resonators are in the range of 1-10MHz. While these exhibit high *Q*s, silicon is still not the most widely used material for timing applications, one of the reasons for this is that it is not easy to go to high frequencies using the Lame mode owing to its size constraints. Furthermore, having a high frequency and thereby decreasing the size of the device would significantly reduce the transduction area resulting in a very large motional impedance. One of the solutions to this is addressed in chapter 4.

While it is possible to fabricate Lame modes using larger gap sizes of 1-2um for frequencies smaller than 10MHz, higher frequency applications would require that the gap sizes be reduced, to improve the motional impedance of the device. Therefore, other than the small transduction area, it is also imperative that these devices have smaller gap sizes, in the range of sub-300nm, since motional impedance is inversely proportional to the square of the gap. This is only possible using the HARPSS process, and there have been several such devices fabricated in the past, using a similar process as described earlier in this chapter. However, since these devices are IP resonators, so if there was a fabrication run only dedicated to these devices alone, we could use the 3-mask variation of the process, that is described in section 2.1. The Figure 12 below shows images of two types of Lame mode resonators with turnover points at 40°C and 45°C. These were measured in the Georgia Tech IMEMS lab for [17].

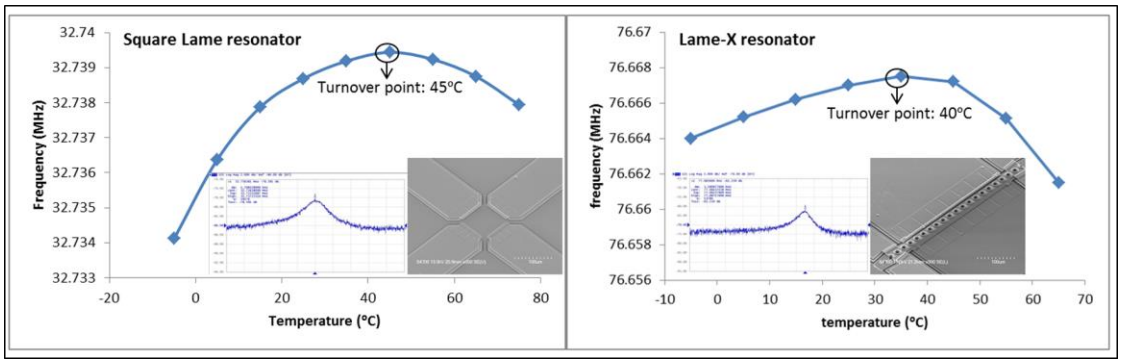

Figure 12 – Square (left) and cross-sectional (right) Lame mode resonators with frequency-temperature turnover points, caused because of highly doped substrates.

In order to use these devices as temperature compensated devices, it also becomes a requirement that there be additional heater elements in the vicinity of the device, to form the heating control system. These heaters may be either shorted to the electrodes to pass current through the device, or may be near the device but not touching it, to heat the device through its surrounding regions, like the handle layer. Figure 13 shows a picture of a heater around the resonator body, that has been fabricated in our research group. It is worth mentioning that these additional features are compatible even with the 3-mask process, since they only comprise of trenches being etched inside the device layer.

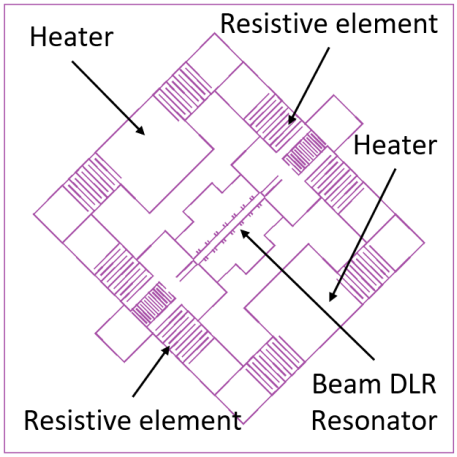

Figure 13 – An example of the trench mask layer of additional heater elements included in the vicinity of a resonator, which are easily enabled by the 3-mask HARPSS process.

The Table 3 below shows the various Lame modes that have been fabricated in silicon in literature. It is important to list these devices, since it can be seen that while high quality factors (thereby high *f.Q* products) have been achieved, most of these resonators are <10MHz. While these devices could be used for lower frequency applications, high frequency applications would still need frequency up-convertors and would result in a large power consumption. Chapter 4 talks about how this is overcome in a high frequency device and the design and fabrication method has been highlighted.

Table 3: List of Lame mode resonators in increasing order of frequency for silicon

Paper	Frequency (MHz)	f.Q (10^{12})	Device material
Hamelin, et al, 2016 [45]	1.61	0.48	Silicon
Lee, et al, 2008 [16]	2.065	8	Silicon
Lee, et al, 2008 [46]	2.18	2.4	Silicon
Khine, et al, 2007 [47]	6.3	10	Silicon
Shao, et al, 2008 [48]	6.35	11	Silicon
Chen, et al, 2015 [49]	10	17	Silicon
Chen, et al, 2016 [14]	10	8.2	Silicon
Niu, et al, 2010 [50]	10.3	2	Silicon
Khine, et al, 2007 [51]	12.9	10.3	Silicon
Ng, et al, 2014 [52]	13	19	Silicon
Heidari, et al, 2011 [53]	37.8	0.378	Silicon
Thakar, et al, 2013 [54]	41.5	16.6	Silicon
Tabrizian, et al 2016 [17]	77	3.3	Silicon

2.4 Multi-transduction integration compatibility

While the HARPSS process has been successfully used over the last few years for fabrication of capacitive devices, one of its drawbacks has been to combine it with other transduction mechanisms, such as piezoelectric or piezo-resistive devices. It is essential to describe this aspect, because many applications require other methods of transduction such as piezoelectric. To truly revolutionize the process, it becomes imperative that it becomes compatible with other materials as well.

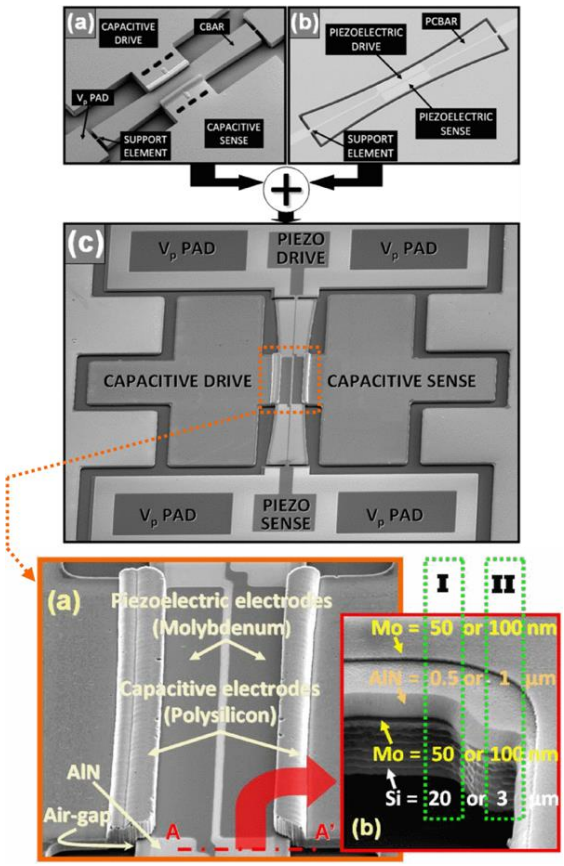

Figure 14 – (top a) Capacitively transduced Concave silicon Bulk Acoustic Resonator (CBAR); (top b) Piezoelectrically transduced CBAR (P-CBAR); (top c) Combined Capacitive and, Piezoelectric transduction for CBAR (C-P-CBAR). SEM images (bottom a) showing close-up of the combined capacitive and piezoelectric transduction, and (bottom b) illustrating the thickness of the piezo-stack for the 20 µm (Type-I) and 3 µm (Type-II) thick C-P-CBAR [32].

One of the main factors that limits this process to capacitive devices only, is the high temperature being used during processing. Many of the steps involve high temperature annealing and oxidation steps at about 1100C. A version of this process was previously carried out using HARPSS process, however, that involved using the metal electrodes and covering them with oxide to protect them at high temperatures [32]. Figure 13 shows images from this process, wherein C-BAR structures had been fabricated using this combined process. High *Q*s of about 10k were measured by this process, however the yield was extremely low, and the drawbacks of the fabrication process are further explained in chapter 5.

Due to its incompatible nature with metal, it becomes obvious that these high temperatures are not suitable for piezoelectric stacks which contain metal electrodes. Another aspect that limits this process to capacitive transduction is the incompatibility in stress levels of the LPCVD polysilicon and piezoelectric metals such as AlN. While the latter can be optimized by careful characterization of the films, the former is a major limiting factor for cross-transduction compatibility. The solution to this aspect has been spoken about in detail in chapter 5, and one combined piezo-capacitive device has been fabricated with appreciable results having a capacitive gap as small as 95nm. A new reduced temperature HARPSS process has been designed for this purpose, and the challenges involved are highlighted in that chapter.

CHAPTER 3. THICK EPI-POLYSILICON FOR ULTRA-HIGH QUALITY FACTOR BAW DISK GYROSCOPES

3.1 Why Epi-poly for High Q BAW Disk Resonators?

SCS disks, both as center and side supported resonators, are commonly fabricated in the <100> SCS substrate, owing to its compatibility with foundry processing and large commercial availability. However, for the N=3 mode, center-supported <100> SCS disk resonators undergo shear motion at the center of the disk due to non-uniform deformation of antinodes caused by material anisotropy as shown in Figure 15. This causes the N=3 mode to suffer from large dissipation through the support, as shown in Figure 17, and also explained later in the chapter. Hence, center-supported disk resonators must contain decoupling structures to improve Q_{ANC} [9], [13]. But the inclusion of such structures also introduces additional thermo-elastic damping, thereby limiting Q to values much lower than the intrinsic Akhiezer limit [9]. Ideally, <111> SCS disks are in-plane isotropic for the n=3 elliptical modes. However, their out-of-plane components are different, causing a large inherent frequency mode split.

Therefore, it is desirable to explore the potential of an isotropic substrate such as epipoly as an alternative material for MEMS BAW gyroscope applications. While it is possible to deposit doped polysilicon using LPCVD process, achievable film thickness is limited by the film stress to less than 10 microns, and devices made from thin films are susceptible to out-of-plane spurious modes. The use of a thick epitaxially grown layer negates these disadvantages and enables in-plane BAW modes that are immune to

influences from out-of-plane spurious modes while providing larger capacitive area for efficient transduction.

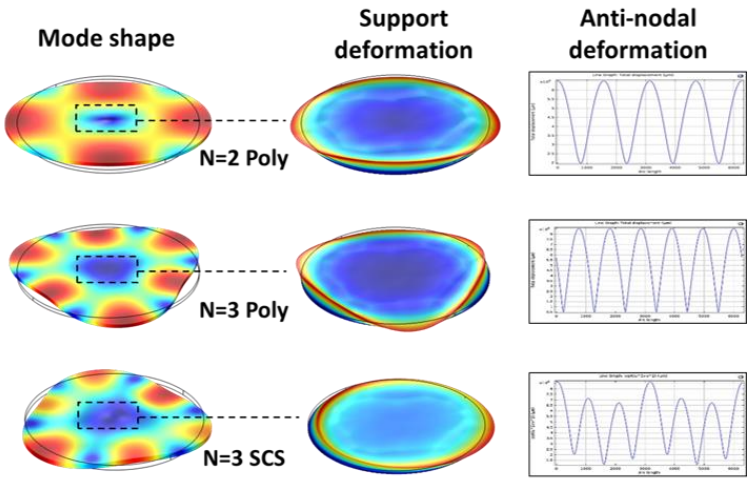

Figure 15 – Comparison between polysilicon and <100> SCS gyroscopic modes in terms of deformation of the center post as a result of anti-nodal deformation. The SCS disk has a shear deformation at the center due to material anisotropy, which increases anchor loss in center-supported resonators.

3.1.1 Anchor-loss in Epipoly BAW Disks

To verify the advantages of the isotropic epipoly substrate, anchor loss for center supported disks are compared for <100>, <111> silicon and epi-polysilicon using finite-element simulations. A 45um thick, 2mm disk was simulated in COMSOL, for different anchor diameters for N=2 and N=3 on polysilicon and N=3 on <100> SCS. The n=2 mode for <100> SCS was not taken into consideration, since the mode is not degenerate due to anisotropy of SCS, and cannot be used for mode-matched gyroscopic applications.

The simulation was done using a perfectly matched layer (PML) [35]. The results are shown in figure 6. The Q_{ANC} for N=3 poly is found to be over 4 orders of magnitude larger than the n=3 in <100> SCS for the same size stem. It also shows a dissipation of over 2

orders of magnitude lower than N=2 modes in poly, which makes N=3 elliptical mode in polysilicon ideal for substrate-decoupled high-*Q* solid disk BAW gyroscopes. This clearly highlights the main advantage of isotropic polysilicon over <100> SCS for both N=2 and N=3 mode shapes. <111> SCS are seen to be in-plane isotropic for the N=3 mode, however out-of-plane displacement components add a large frequency split between the modes (~4kHz) even without considering crystallographic misalignments (Figure 16). The <111> SCS N=2 elliptical mode is also degenerate, however small OOP crystallographic misalignments of +/-0.5° can increase the mode splits by ~7kHz. Hence, <111> SCS is not the most suitable substrate for implementation of gyroscopic BAW resonators. Furthermore, it is possible to attain high quality factors for epi-polysilicon using large support diameters, which are more suited for gyroscopic applications to allow better out of plane insensitivity, as compared to SCS. In this work, we have used a large support diameter of 200µm for a 2mm diameter disk.

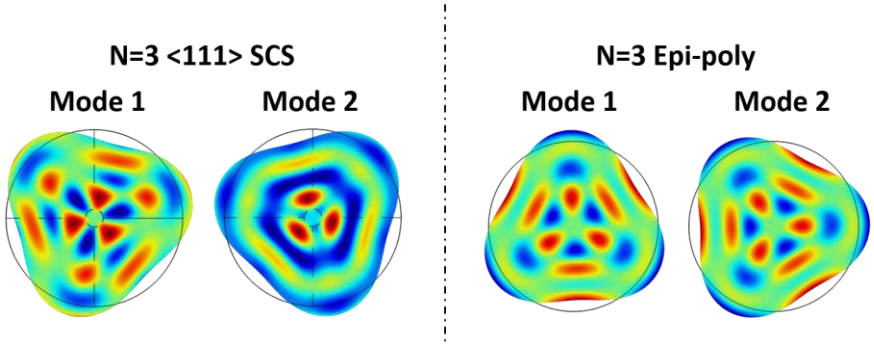

Figure 16 – Comparison of N=3 mode shapes for <111> SCS (left) and epipoly (right).

Another advantage of using epi-polysilicon over SCS is the higher quadrature isolation in in-plane gyroscope applications. It is explained in the later sections that due to symmetricity of the mode shape, we get much lower isolation levels as compared to

asymmetric <100> SCS. This means that the quadrature is more isolated from the gyroscope signal thereby reducing ΔQ between the mode shapes, which in turn helps reduce mechanical noise and improve gyroscope performance. Keeping these factors in mind, we can design both N=3 and N=2 BAW disk gyroscopes in epipoly, the details of which are explained in the next two sections.

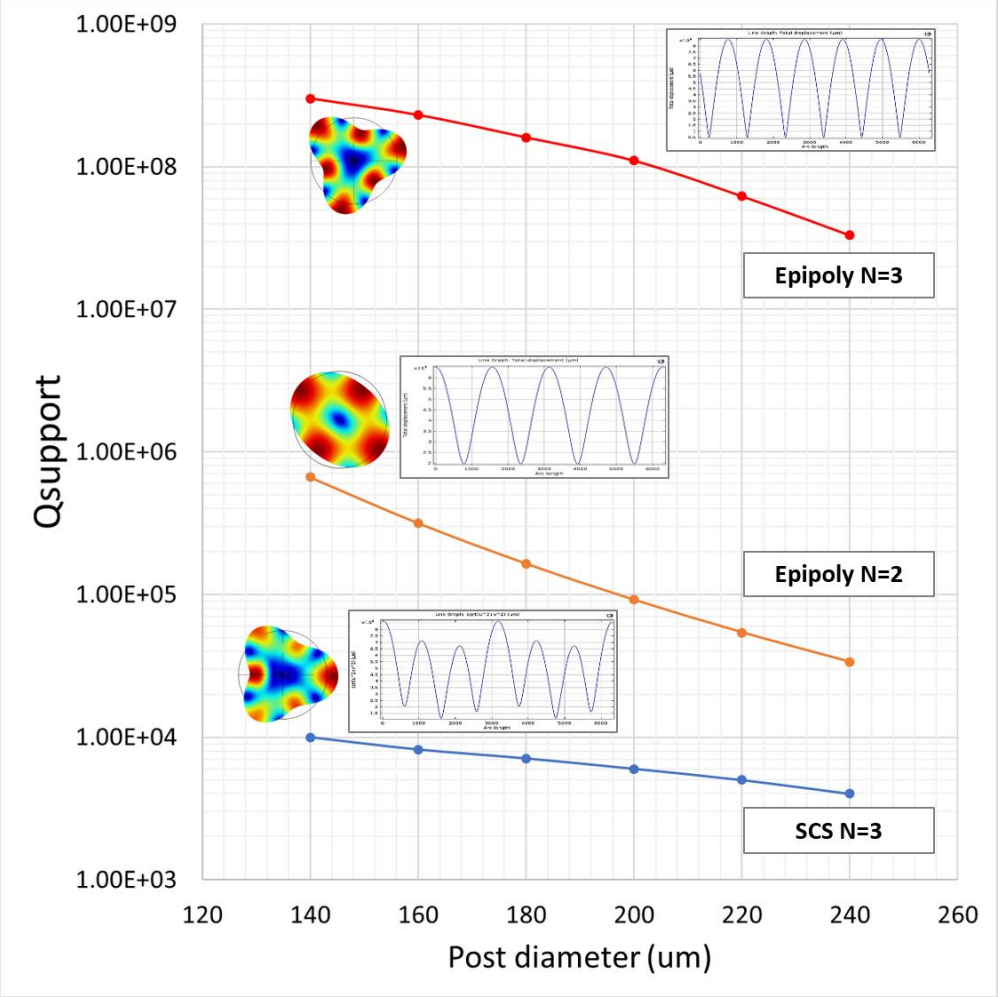

Figure 17 – Simulated Q_{ANC} for SCS and epipoly mode shapes for fully solid disks and the arc length for the mode shapes about the center (inset graphs).

3.2 Third Elliptical Mode (N=3) Epi-poly BAW Disk Gyroscope Design

An in-plane BAW disk gyroscope was designed for the epipoly substrate using COMSOL. A frequency of 3.15MHz was chosen for a diameter of 1.88mm, since SCS disks having the same frequency had been successfully tested in the past using similar dimensions, and also to reduce the effect of the closest spurious modes to the disk, which is explained later in this section. A spring-like decoupling structure as shown in Figure 18 was chosen, to decouple the disk further from the center support and to allow an even larger Q_{ANC} for the disk. While epipoly N=3 modes inherently show the lowest anchor loss, as shown in Figure 17, there would be fabrication variations within the design which would degrade Q_{ANC}. Hence, we have to design the decoupling springs in such a way that they allow the disk to have a large post size, yet they do not deteriorate the TED losses in the substrate. Owing to the large post size, the disk can also be wirebonded to the center directly, which reduces the steps in the fabrication process. Figure 18 shows the N=3 mode shapes and the decoupling notches, with the backside holes. The decoupling spring was designed having the same initial trench width as the trenches defining the resonator. The backside holes are spoken about in detail in section 3.3.4. Various aspects were taken into consideration while simulating the disk resonator, such as the mode-split across fabrication variations of trench variation, trench sloping and mask ovalness. Spurious modes across thickness variation were also considered, this proved to be a lot harder to simulate considering the large thickness variation across the epipoly substrate which was as large as 5um across the wafer. Table 4 shows the designed parameters for the epipoly BAW gyroscope.

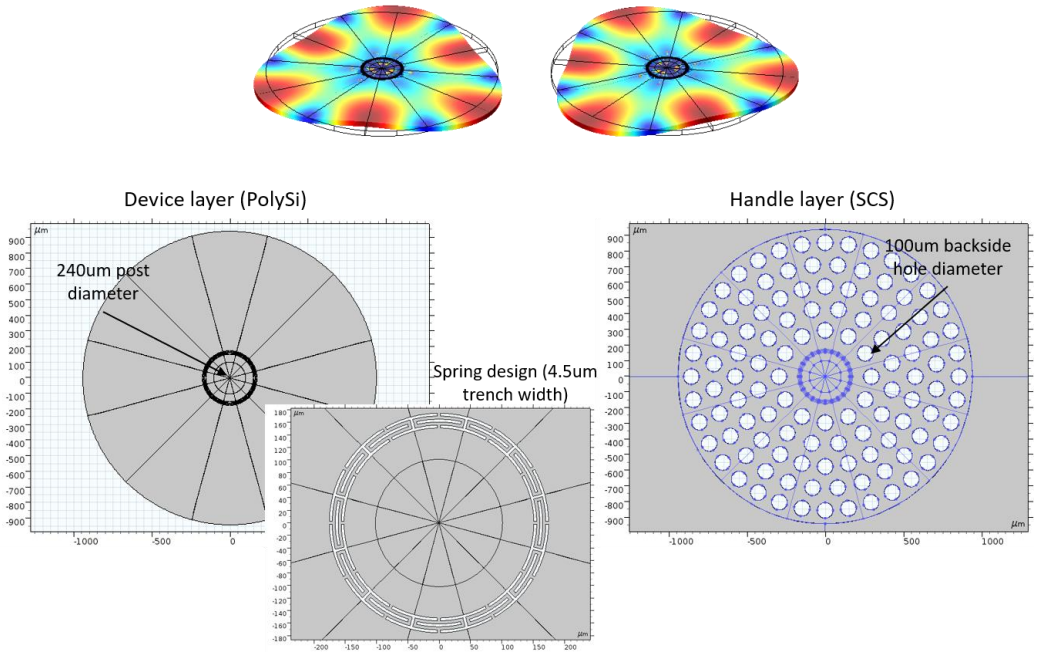

Figure 18 – The N=3 degenerate mode shapes for the epipoly disk (top), the decoupling spring on the device layer and the backside holes on the handle layer (bottom).

Table 4: N=3 Epi-polysilicon BAW gyroscope parameters

Parameter	Value
Diameter (um)	1880
Gap g_0 (nm)	350
Drive amplitude (nm)	35
Mass M (ug)	112
Angular gain Ag	0.23
Electrode Area A (um^2)	11074
Quality factor Q	1M
Polarization voltage Vp (V)	25
Frequency f_0 (MHz)	3.15
SF (nA/dps)	16.86

MNEA (°/h/√Hz)	0.36
ENEA (°/h/√Hz) @I_n = 1pA/√Hz	0.21
TNEA (°/h/√Hz)	0.42
ARW (°/√h)	0.007

The Akhiezer limit in polysilicon is not very well known, hence was assumed to be the same as that of SCS silicon. However, a quality factor of 1M was assumed for the device, considering the TED losses due to the spring design and also the Akhiezer limit. Another reason for choosing decoupling springs besides further improving Q_{ANC}, was to make the total quality factor TED limited, since TED loss limited devices have been shown to measure more consistent quality factors as compared to anchor loss limited *Q*s, as those are not dependent on external factors such as wirebonding, mounting on the PCB and other sources which cannot be simulated accurately.

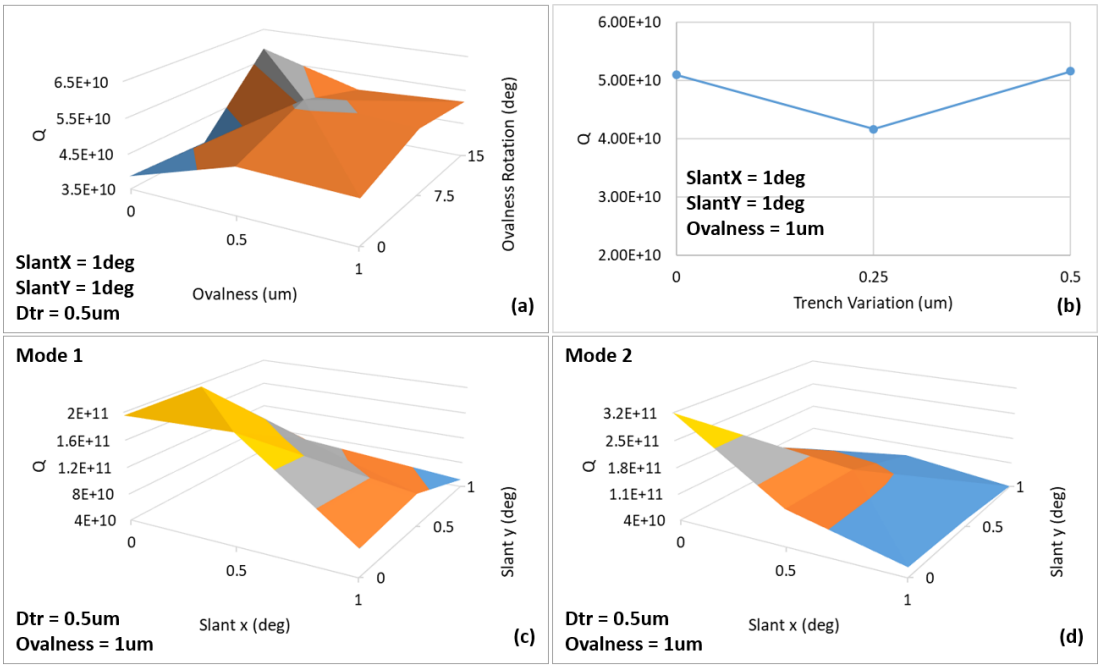

Figure 19 – Q anchor variations for N=3 epipoly design using worst case corner variations of 1° sidewall slanting, 0.5um trench variation and 1um ovalness. (a) shows

variation w.r.t ovalness and direction of ovalness, (b) shows variation over trench width, and (c) and (d) show variations over sidewall slanting in x and y directions for both the modes. It is seen that the sidewall slant is the factor that affects the Q_{ANC} of the N=3 epipoly design the most.

3.2.1 Simulations over Fabrication Variations

As stated earlier, it is critical to simulate the quality factor and the frequency change of the disk for commonly occurring fabrication variations. While the simulations to determine anchor loss and TED can be done easily in COMSOL, these must be swept over certain variances in parameters to figure out if the disk can work practically after fabrication. While the ideal device can be simulated to show a Q_{ANC} of over 100B, simulating over these variations shows a drop in Q_{ANC}. The fabrication or corner variations that were considered were a 0.5um trench width variation, 1° sidewall slant in both the x and y direction and a 1um ovalness in the shape of the disk. While the trench width and ovalness might come from the lithography of the wafer, the sidewall slanting comes from the nature of DRIE etching, wherein the gases enter the trenches at a small angle towards the wafer edge because of the angle created by the showerhead which is only at the center inside the etching chamber. Figure 19 shows the simulated variations for the epipoly disk from these variations, and the overall Q_{ANC} reduces to 35B across all the variations. It is also noted that while the ovalness and trench width of the decoupling structure don't affect the Q much, the major loss comes from the sidewall slanting. In comparison, if we do the same simulations for an SCS disk with the same dimensions, we see that not only is the Q_{ANC} heavily damped by the variations, but also create a large mode split of about 450Hz. The Q_{ANC} for SCS in these simulations is as low as 11M across these variations, as shown in Figure 20.

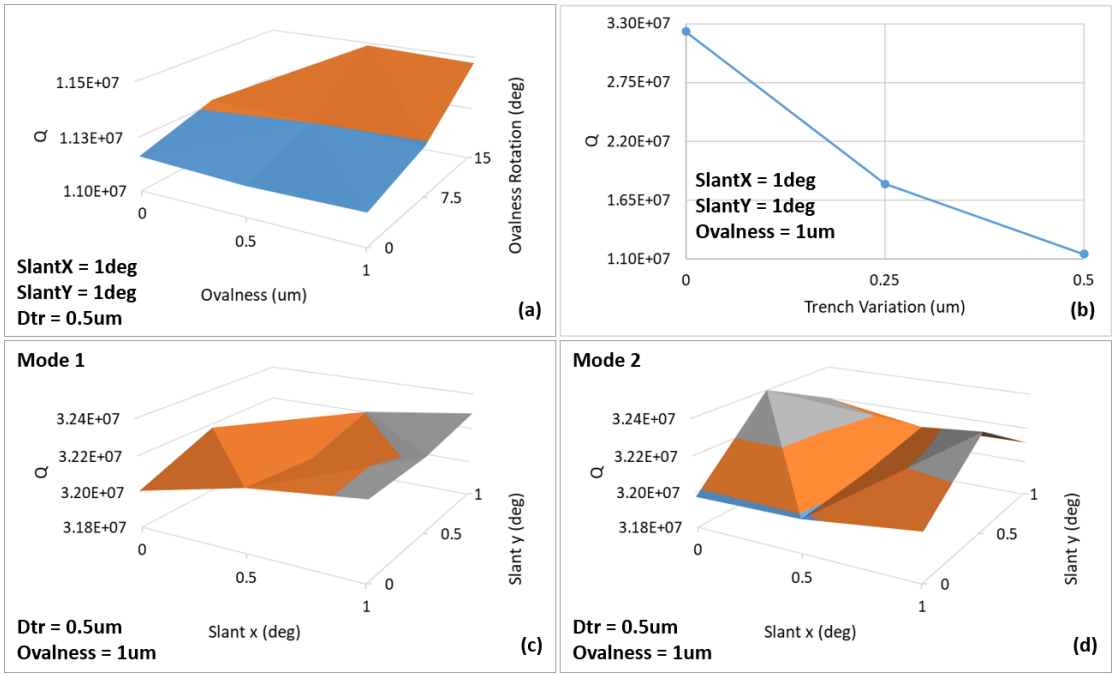

Figure 20 – Q anchor variations for N=3 SCS design using worst case corner variations of 1° sidewall slanting, 0.5um trench variation and 1um ovalness. (a) shows variation w.r.t ovalness and direction of ovalness, (b) shows variation over trench width, and (c) and (d) show variations over sidewall slanting in x and y directions for both the modes. It is seen that the trench variation is the factor that affects the Q_{ANC} of the N=3 SCS design the most, however as stated earlier, Q_{ANC} for SCS disk reduces to 11M.

The designed disk at 3.15MHz has two spurious modes, at about 2.86MHz and 3.28MHz, so it should be taken care that these modes do not interfere with the degenerate mode shapes of the disk. The frequencies of these spurious mode might shift if fabrication imperfections are considered, and should be designed such that they are far apart from the frequency in interest. Because of the isotropic nature of the epipoly substrate, we can see that the fabrication variations do not in fact, cause these spurious modes to shift the frequency by a lot. Figure 21 shows the change in spurious mode frequencies, with change in trench variation considering a 1° sidewall slanting (which is an extreme case), and also for thickness variations. While trench variations do not affect the frequencies much, we see a

large change in spurious mode frequencies from the wafer thickness variation. This is one disadvantage of the epipoly substrate, wherein a large thickness variation exists in commercial wafers. Such a large thickness variation would not exist in SCS SOI wafers.

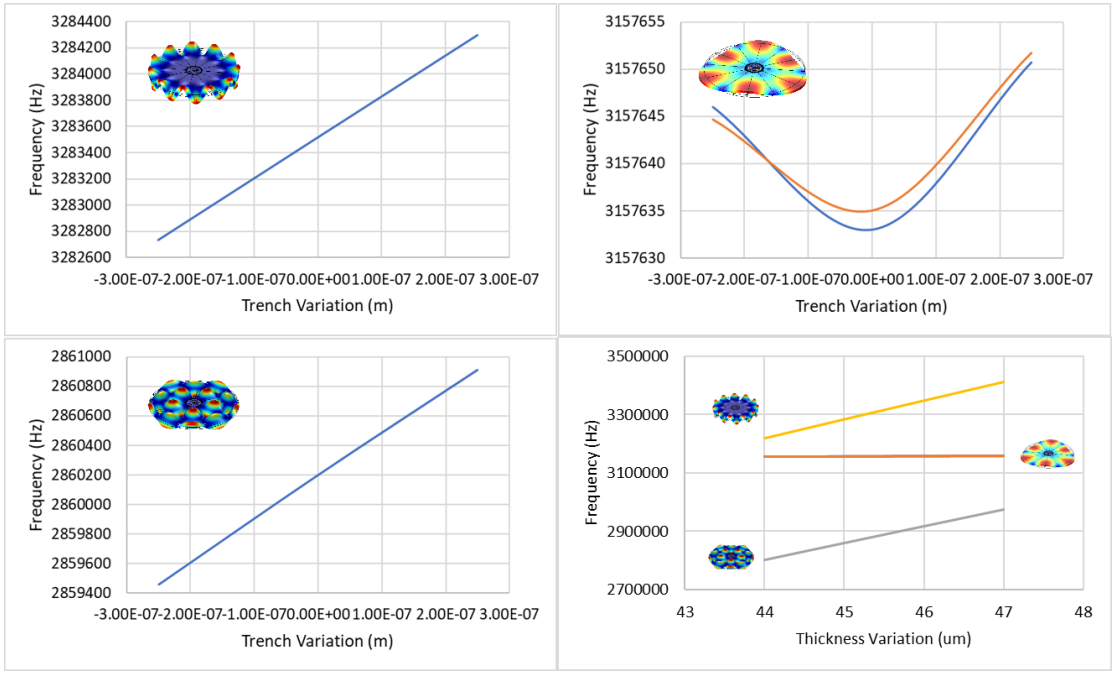

Figure 21 – Frequency variations for the spurious modes and the n3 modes for trench and thickness variation of the substrate. We can see that the thickness variations affect the spurious modes much more than the trench variations, since they contain OOP components. The in-plane n3 mode however, remains largely unaffected by thickness variation.

Once the spurious modes are simulated, it becomes essential to also simulate the change in quality factor because of fabrication imperfections. In this design, the Q_{ANC} is extremely large owing to the decoupling springs, so the fabrication variations have little impact on the anchor loss. However as stated earlier, the addition of these springs introduces a TED loss in the disk. While the Q_{TED} is simulated to be reasonably large >7M, it becomes imperative to sweep the Q_{TED} over the same variations as the spurious modes. Figure 22 shows the changes in Q_{ANC} and Q_{TED} over trench variations, while considering a

1° sidewall slanting. It should also be noted that this 1° sidewall slanting was assumed for all the fabrication variation simulations which was an extreme case, and the actual expected change in spurious modes and quality factors would hence be much lesser than simulated.

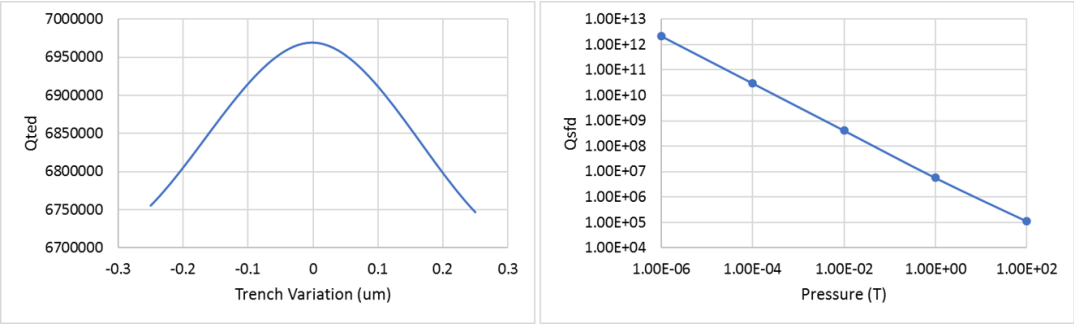

Figure 22 – Variations of Q_{TED} (left) over +/-0.25um trench variations and Q_{SFD} (right) for N=3 epipoly BAW gyroscope.

The effects of anisotropy of SCS are evident in the comparison between the isolation levels of epipoly and SCS N=3 modes. In a gyroscope, it is important to have a small or negligible cross-coupling between the drive and sense modes, since we do not want interference of the drive mode while sensing the output current. The level of isolation between the modes also in turn means that the gyroscope would not drift as much which results in better bias instability for the gyroscope, which is a high performance metric of its design. In SCS, the fabrication variations add a large in-phase cross coupling between the two modes, and also considering the inherent anisotropy of the material as stated earlier, results in its slightly asymmetric mode shape, even in the presence of decoupling notches. Hence, on simulation of the isolation levels, which is the ratio of the sense output to the drive for zero rotation, we see a much lower isolation level for SCS of 62dB, as compared to epipoly, which is 78dB for N=3 mode shape (figure 17). This further proves the benefit of using epipoly for N=3 gyroscopes, over SCS.

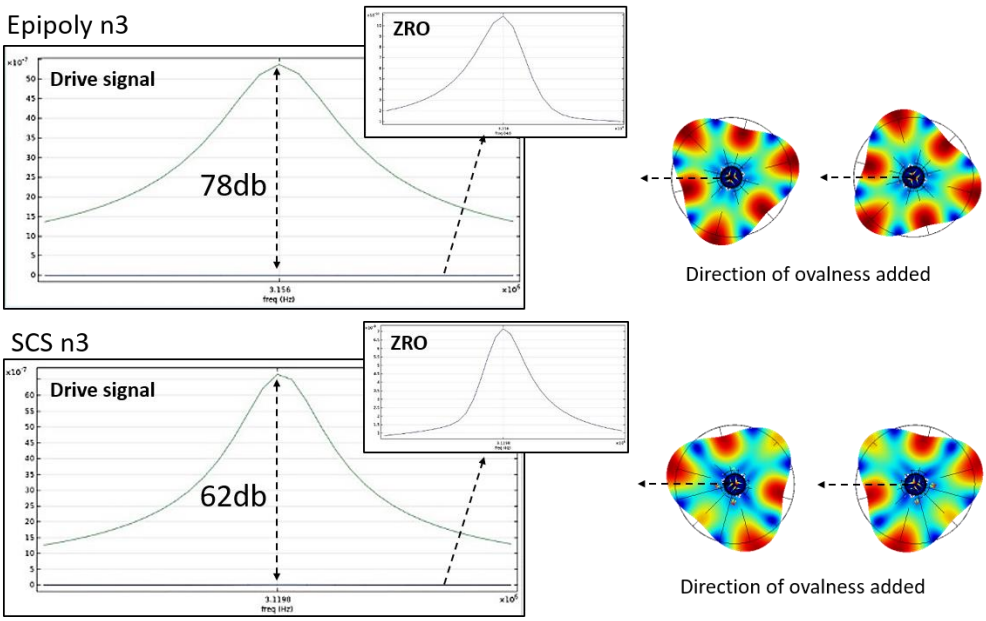

Figure 23 – Simulated isolation level for N=3 mode of epipoly (top) as compared to SCS (bottom), over fabrication variations. The animations on the right show the direction of maximum ovalness added to the simulation, exactly between the two mode shapes.

3.3 Second Elliptical Mode (N=2) Epi-poly BAW Disk Gyroscope Design

While the N=3 mode epipoly BAW gyroscope clearly shows improvement over SCS in terms of higher *Q*, better isolation and less susceptibility to fabrication variations, the epipoly substrate can also be used to design a gyroscope using the N=2 degenerate mode shape. This cannot be done in SCS substrates, as the N=2 mode is not degenerate for a solid disk resonator due to its anisotropy. An N=2 gyroscope was designed at 1.5MHz using the similar decoupling springs as the N=3 design, however, they were now symmetric to the 45° mode shapes. Figure 24 below shows the mode shapes and the dimensions and symmetry of the disk and its decoupling spring. A disk radius of 1140um was chosen, such that the spurious modes around the N=2 mode were not in its proximity. Also, using a

larger outer diameter by keeping the inner spring diameter to be the same as the N=3, we can improve Q_{ANC} in the N=2 design.

3.3.1 Modified Electrode Arrangement

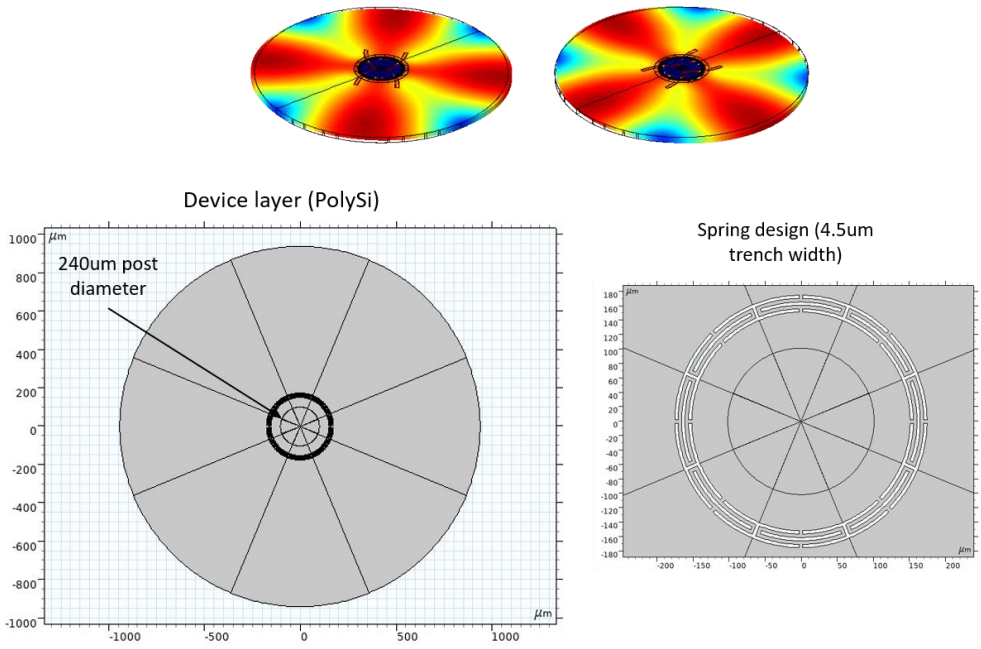

Figure 24 – The N=2 degenerate mode shapes for the epipoly disk (top), the decoupling spring on the device layer (bottom).

Ideally, the N=2 design should allow even better isolation and larger scale factors owing to larger transduction area because of the inherent mode shape in the disk. If we were to have the same electrode symmetry for the N=2 design as the N=3 shown in the previous section, it would consist of a total of 16 electrodes as compared to 24 electrodes for the N=3 gyroscope, because the antinodes are now at 45° angles as compared to 30° earlier. This increases the transduction area of each electrode, even though the effective transduction area within the electrode is not present in its entire electrode span. However,

we have to change the electrode design for the N=2, since the antinodes at opposite electrodes are in-phase (out-of-phase for N=3), which does not provide us with a differential output. If we were to use the electrodes at 90° to each other which are indeed out-of-phase, for sensing, then we cannot have tuning electrodes for the sense mode since there are no more antinode locations for that mode. Hence, we need to modify the electrode structure, wherein we use the span of one 22.5° electrode and split it into both, the sense out and two tuning electrodes on either side. This modified electrode design is explained in Figure 25. In the figure, VT1 corresponds to the tuning locations of drive (D) and VT2 corresponds to those of the sense (S). In the figure on the left, we see that using the regular arrangement, we cannot get access to a differential location since both the S electrodes are in-phase. Note that if we split the S electrodes, we also need to split the D electrodes to allow for symmetry in the disk, as having electrode asymmetry might lead to a small mode split while applying dc voltages to the disk, and also might lead to an imbalance of voltages causing the disk to pull-in in the worst case. In the simulated modified electrode design, the S and D electrodes are now made 10° each and the two tuning electrodes VT1 and VT2 on either side are 6.25° each. These numbers are chosen to make sure that the transduction area of the sense out is not reduced drastically, yet we have enough electrode area for the tuning mechanism.

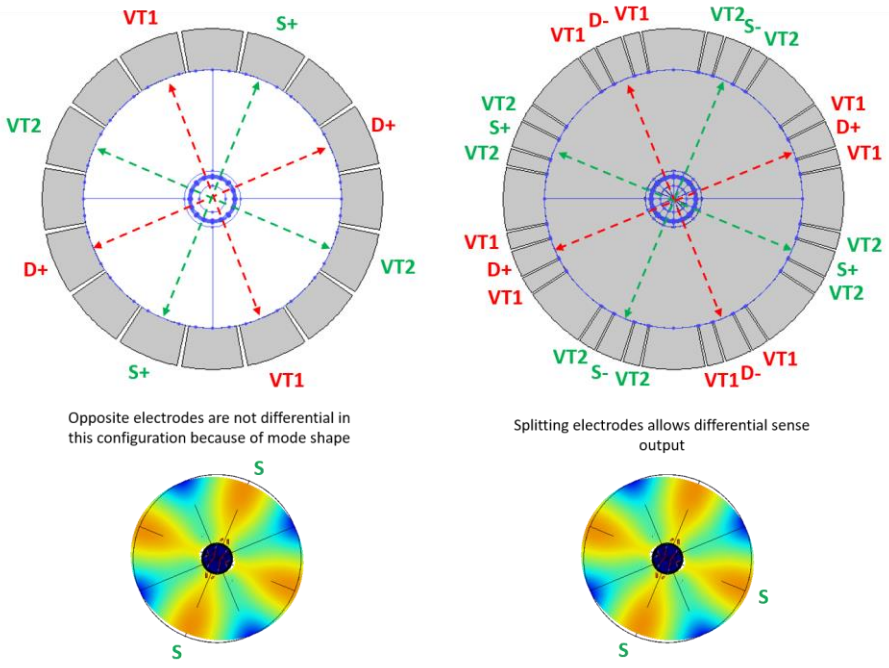

Figure 25 – Regular (left) and modified (right) electrode arrangement for the N=2 mode. By splitting the original sense electrode into one sense and two tuning electrodes, we can achieve a differential operation for sense out as well as tuning facility for the sense mode. Drive mode also has to be similarly split for symmetry.

3.3.2 Simulations over Fabrication Variations

Similar to the N=3 design, we must simulate the N=2 design over the similar fabrication variations as was done in section 3.2. For the current dimensions of the disk, the Q_{ANC} simulated for the ideal case was close to 4B. However, we must consider fabrication variations of 0.5um in trench width, 1° sidewall slant and 1um of ovalness. In the N=3 design, we see that it is primarily the ovalness and the direction of ovalness with respect to the mode shapes that causes the major dissipation in the anchor and reduces Q_{ANC}. However, for the N=2 disk, we see that all the three fabrication variations play a role in the drop in the Q_{ANC}. While the drop is not as significant for this design, the Q_{ANC} is

decreased to a value of 1.1B, which is still 3 orders of magnitude higher than the Q_{TOT} that the disk is designed for. The anchor loss simulations for N=2 are shown in Figure 26.

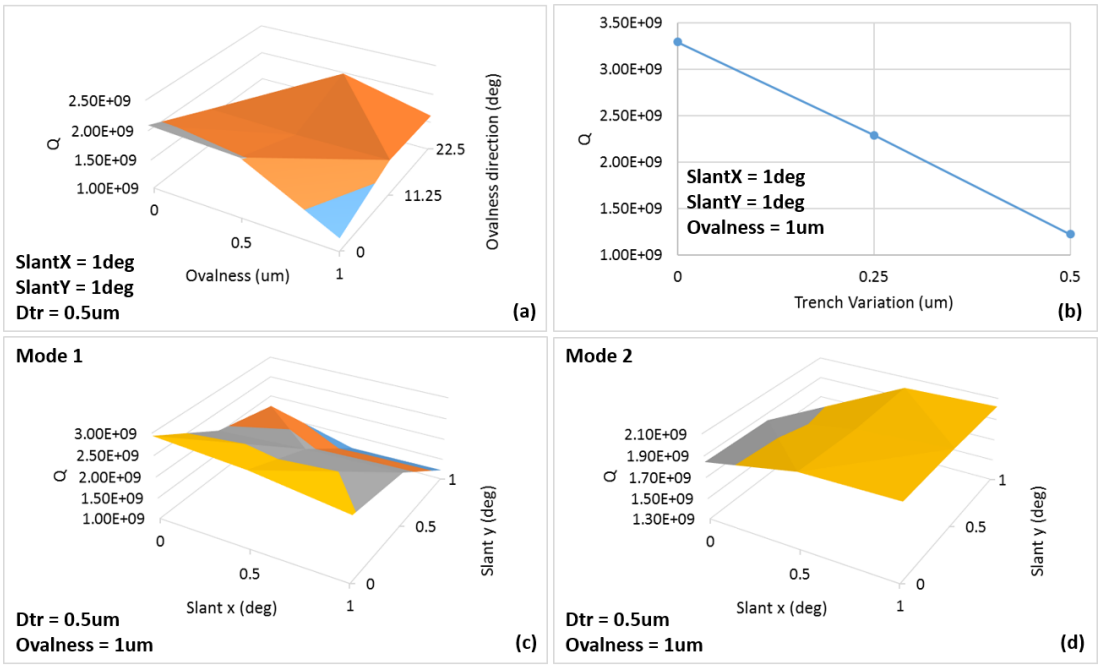

Figure 26 – Q anchor variations for N=2 epipoly design using worst case corner variations of 1° sidewall slanting, 0.5um trench variation and 1um ovalness. (a) shows variation w.r.t ovalness and direction of ovalness, (b) shows variation over trench width, and (c) and (d) show variations over sidewall slanting in x and y directions for both the modes. It is seen that all the variations affect the Q_{ANC} of the N=2 epipoly design, dropping its value to 1.1B.

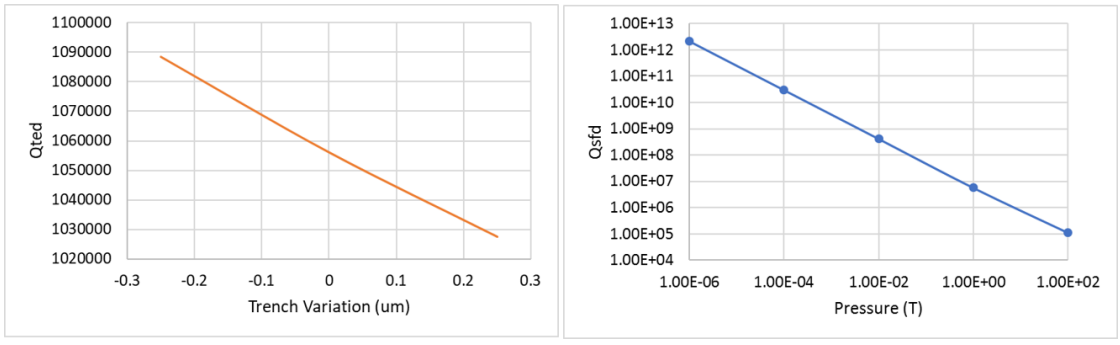

Figure 27 – Simulated Q_{TED} and Q_{SFD} for N=2 epipoly disk. The total Q will be limited by TED which is about 1M across trench variation.

While the Q_{ANC} is reasonably high for the N=2 design, the decoupling springs become more compliant because of the larger angle between the two modes, making them displace larger. We see that this phenomenon causes more thermoelastic damping in the disk and reduces Q_{TED} of the device. Even though sidewall slanting and ovalness show negligible change the Q_{TED} of the device, the simulations for TED using trench variation of 0.5um show that the minimum quality factor is around 1M. This value limits the Q_{TOT} of the device, making it TED limited. The simulation of TED over trench variation is shown in Figure 27.

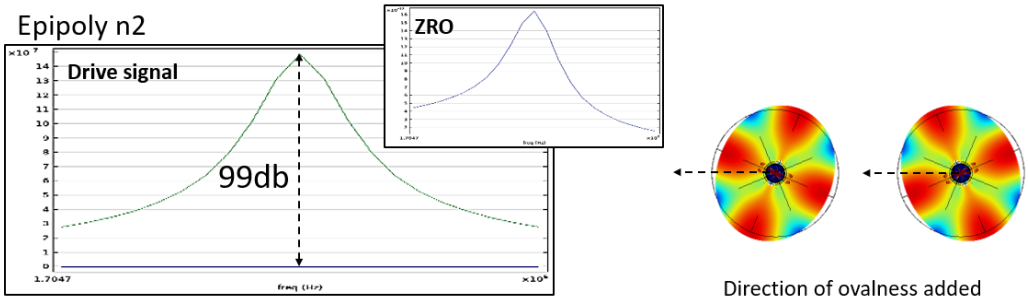

Figure 28 – Simulated isolation level of 99dB for N=2 mode of epipoly disk over fabrication variations. The animations on the right show the direction of maximum ovalness added to the simulation, exactly between the two mode shapes.

Isolation simulation of N=2 mode shows better readings than N=3 epipoly. This is due to the larger displacement of the mode shape, which causes less in-phase coupling between the two modes. Even considering corner variations, the simulated isolation levels for N=2 design are as low as 99dB. Hence, for very low bias drifts, N=2 design might be the most suited, provided the frequency split is small. Figure 28 shows the simulated result for the isolation, whilst considering the ovalness direction exactly between the two modes in the worst case condition.

After running the various simulations over fabrication variations, we can calculate the different parameters of the gyroscope using the value of the total quality factor that is expected. Table 5 gives the calculated parameters for N=2 gyroscope.

Table 5: N=2 Epi-polysilicon gyroscope parameters

Parameter	Value
Diameter (um)	2280
Gap g_0 (nm)	350
Drive amplitude (nm)	35
Mass M (ug)	140
Angular gain Ag	0.46
Electrode Area A (um^2)	16116
Quality factor Q	1M
Polarization voltage Vp (V)	25
Frequency f_0 (MHz)	1.5
SF (nA/dps)	29.84
MNEA (°/h/√Hz)	0.35
ENEA (°/h/√Hz) @I_n = 1pA/√Hz	0.12
TNEA (°/h/√Hz)	0.37
ARW (°/√h)	0.006

3.4 Reduced-temperature Process for Epi-poly BAW Gyroscope

To experimentally verify the high *Q*s, epitaxially grown polysilicon-on insulator (pSOI) wafers are purchased commercially. An as-grown layer of epi-poly >50μm was polished down to 45μm to create a smooth surface with low roughness. The pSOI device

layer parameters are given in table 1. Solid disk resonators are fabricated in epi-poly using a two-mask process with backside release holes. The elimination of release holes in the disk offers very low TED, combined with the low support loss of the isotropic material, allows the disk resonators to reach Akhiezer limit. Large 2um gaps are etched by DRIE for capacitive transduction in the resonators to ensure fabrication simplicity.

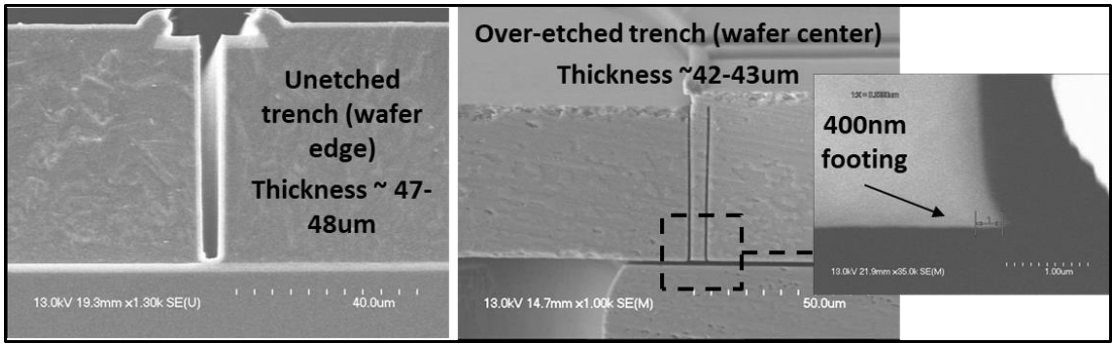

Figure 29 –Different trench etching depths due to a large thickness variation across the wafer, leading to inconsistencies in trench etching.

However, for gyroscopic applications, smaller gap sizes are required to provide full mode-matching coverage over fabrication variations. For this, the HARPSS process, which has been used previously to enable sub-micron gaps for MEMS BAW devices [55], [56], is modified and adapted for the polysilicon. Conventional HARPSS processes involve oxidation and annealing at high temperatures of 1100°C. Despite containing lower residual stress than LPCVD films, epitaxially grown polysilicon is not suited for high temperature processing. For this purpose, a reduced-temperature HARPSS process must be developed to fabricate the disk resonators, so that large stress is avoided in thick epi-poly films during high temperature processing [57]. The wafer specifications of the epi-poly substrates are shown in Table 6.

Table 6: Epi-polysilicon SOI wafer specifications

Parameter	Specification
Device layer	Epi-polysilicon
Thickness (um)	45 +/-2.5
Resistivity (ohm-cm)	0.01-0.05 [P/B]
Stress (MPa)	+/-10
Roughness (um)	<0.1
Surface finish	Polished
BOX layer	Silicon Oxide
Thickness (um)	1.5-2
Handle layer	Single-crystal Silicon
Wafer size (inch)	6 (JEITA std.)
Crystallization method	CZ
Thickness (um)	400
Resistivity (ohm-cm)	0.01-0.05 [P/B]
Surface orientation	(100)
Backside finish	Polished

3.4.1 Low-scallop Low-footing DRIE

One of the major issues with working with epi-poly substrates is the large thickness variation across the wafer. It can be as large as +/-5um across the entire wafer, as shown in the wafer specifications in Table 6. While this thickness variation in the out-of-plane direction can be taken into consideration in device design and is not critical to the efficient working of the device owing to its in-plane resonance modes, it becomes challenging to maintain uniform yield from fabrication, primarily the DRIE process while etching

trenches. Since the exact thickness varies largely across the wafer, it is extremely difficult to know what thickness the recipe needs to be run for, the result of which causes non-uniform trench etching. This leads to some trenches being over-etched, resulting in large footing at the bottom of the trench, while some trenches do not get etched fully. This is shown in Figure 29. One way to resolve this, is to over-etch all the trenches till the whole wafer is etched, but this would increase the lateral etch at the bottom of the BOX layer, thereby increasing the footing which will hamper device operation.

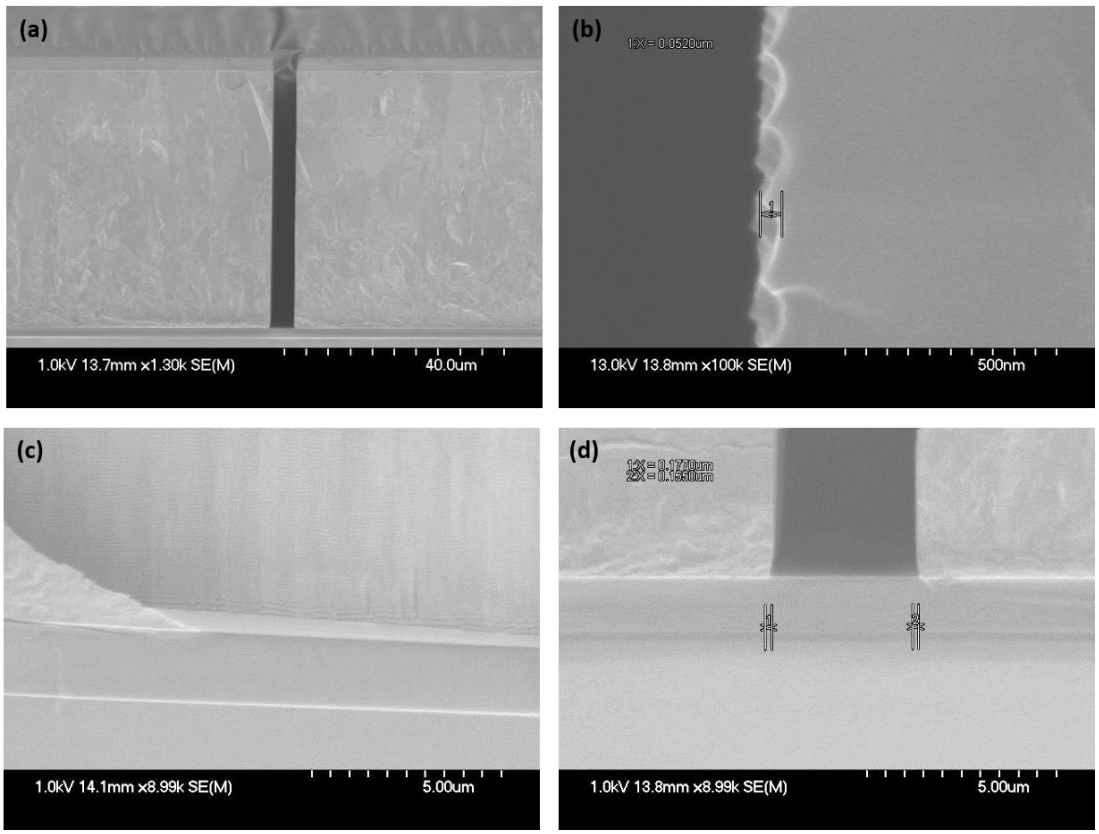

Figure 30 – Improved low-scallop, low-footing trench etching recipe for epipoly wafers. This achieves a state-of-art scalloping of as low as 50-60nm (b) and also low footing of about 150-250nm (d) despite over-etching of trenches. (a) shows a 4um wide trench while (c) shows the trench from its side.

The solution to this issue, is to develop a low-footing recipe, which would allow for over-etching of the trenches, but not result in an increase in footing. Footing is primarily caused because of the accumulation of ions from the etching gases at the bottom of the trench, which cause the trench to etch laterally. Hence, if we can develop an etching recipe which mitigates this, we can also mitigate the footing. One way to do this, is to etch the trench very slowly. This means that the cycling between the etch and passivation cycles should be fast, not allowing the ions of the respective cycles to accumulate at the bottom of the trench. The STS HRM tool is used for this purpose. In the newly developed recipe, we use etch and passivation times to be as low as 4s and 2s respectively. Fast cycling between etching and passivation, also results in small scalloping (Figure 30), which is beneficial for the nano-gaps in the HARPSS process. The etching parameters for the recipe are shown below in Table 7.

Table 7: Low-scallop, low footing trench etching recipe in STS HRM

Parameter	**Value**	
	Etch	Passivation
Cycle time (s)	4	2
Throttle mode, position (%)	Manual, 83	Manual, 83
Gases (sccm)		
C_4F_8	0	200
SF_6	200	0
O_2	20	0
13.56MHz Coil power (W)	2000	1200
LF Platen power (W)	80	0
Platen power ramp (W/min)	0.05	0.06

The results that were achieved from the new recipe are shown in Figure 30. State-of-art scalloping was achieved from the STS HRM tool, with a scalloping size of as low as 50-60nm. This was because of the fast changing of the etch and passivation cycles. The trenches, even after over-etching, had a footing of between 150-200nm, which is reasonable considering a 5um thickness variation across the wafer.

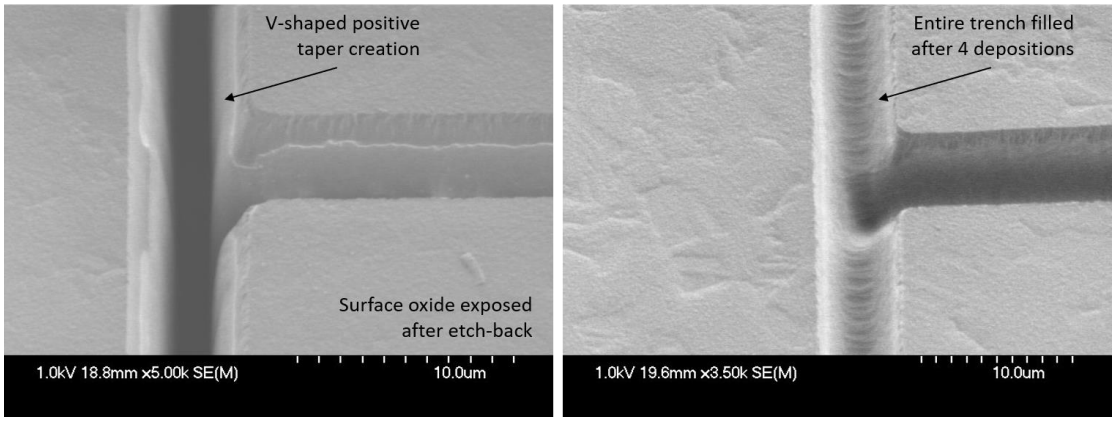

Figure 31 – V-shaped positive taper created in the poly refill after the first poly etch-back (left), and the same trench filled after 4 poly depositions and etch-backs (right).

3.4.2 Poly Etch-back Steps

One of the main steps involved in this process, or any HARPSS process, are the LPCVD polysilicon filling and etching back steps. The etch-back steps however, are important, because while they are simply only Si etching, there are some key parameters involved in them. The main idea of doing a poly etch-back step, is to open out any pinch-offs that are formed at the top of the trench during the poly fill step. The second reason is to simply remove the polysilicon deposited on the surface prior to the next poly deposition so that there is no stress build-up of excess polysilicon. The etch-back should be done both on the front and back of the wafer, for this purpose.

The STS HRM tool was used to etch the polysilicon during these steps. It is important to note that this recipe does not involve a passivation step, just a blank etching step. However, it is essential that this is done by dry etching, since we want the etch to be directional otherwise the polysilicon inside the trenches would also be etched. The etching should be done until there is a formation of a V-shape in the opening of the trench, to make the profile of polysilicon inside the trench to be positively tapered, in order to minimize or completely remove the formation of voids during various poly refills, as shown in Figure 31. The recipe is given in below:

Table 8: Polysilicon etch-back recipe in STS HRM

Parameter	Value
Cycle time (s)	40 (1.5um of poly)
Throttle mode, position (%)	Manual, 90
SF_6 (sccm)	260
13.56MHz Coil power (W)	2000
HF Platen power (W)	30

3.4.3 Stress Mitigation in Epipoly Substrates

For thick epi-poly substrates, another issue is the large residual stress in the wafers and the compatibility with deposition of various materials during processing, primarily LPCVD polysilicon and PECVD oxide. While these depositions are carried out at relatively lower temperatures, they could still affect the overall stress of the wafer. Another aspect that might impact stress is the nature of the pSOI in itself, since the handle layer is made

out of SCS. Furthermore, high temperature processes at 1100°C like oxidation, result in the in absorption of oxide ions into any exposed epi-polysilicon substrate, thereby resulting in a heavily stressed material, which might be visible in terms of wafer bowing. The preliminary process was carried out just like the regular HARPSS process, using high temperature processing for oxidation in terms of the initial oxide mask and also the sacrificial oxide used for the nano-gaps. This caused a large stress on the wafer, which resulted in the wafer being bowed. The process was nevertheless completed on the bowed wafer; however, it was seen that after releasing the devices, they were bent, touching the BOX layer, which proved detrimental to the overall yield of the process. This is shown in Figure 32.

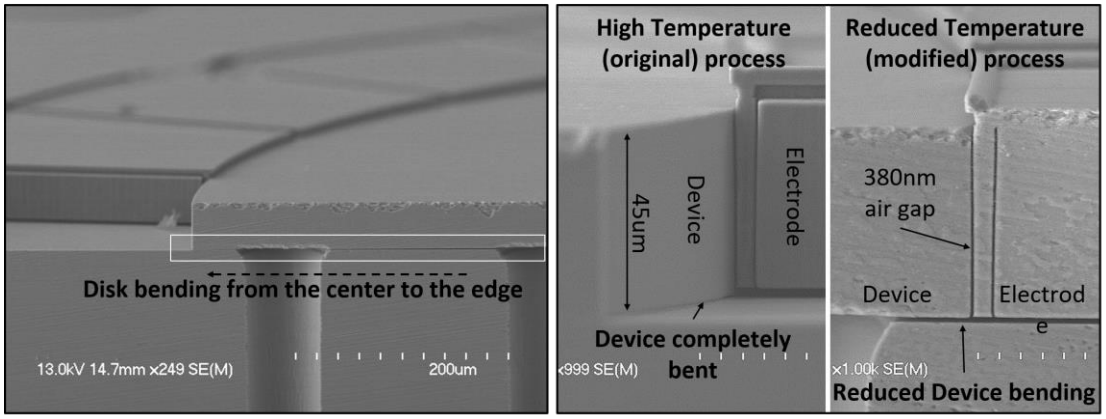

Figure 32 – High temperature processing results in disk bending after device release (left), comparison between high temperature, standard HARPSS process and reduced temperature process (right), resulting in negligible bending for the reduced temperature process.

3.4.4 Backside Hole Etching

In order to fabricate solid disk structures in epi-poly substrates, it is required that the devices be released from the backside of the wafer, ie the handle layer. While this process

might be seemingly easy to carry out, there are some tricky aspects that need to be addressed. One of these aspects is to ensure clean, high aspect ratio trenches, which is not easy to etch considering the large depth of the handle layer which is about 400-450nm. The reason very clean trenches are needed, is because if the trench sidewall quality is bad, it might result in silicon striations which might fall off the sidewalls during the release process and settle randomly at various parts of the device, including between the device and handle layer. This would create a shorting between them, and also reduce the quality factor of the device. Such residues falling between the device and handle layer are hard to spot and clean and can heavily impact yield.

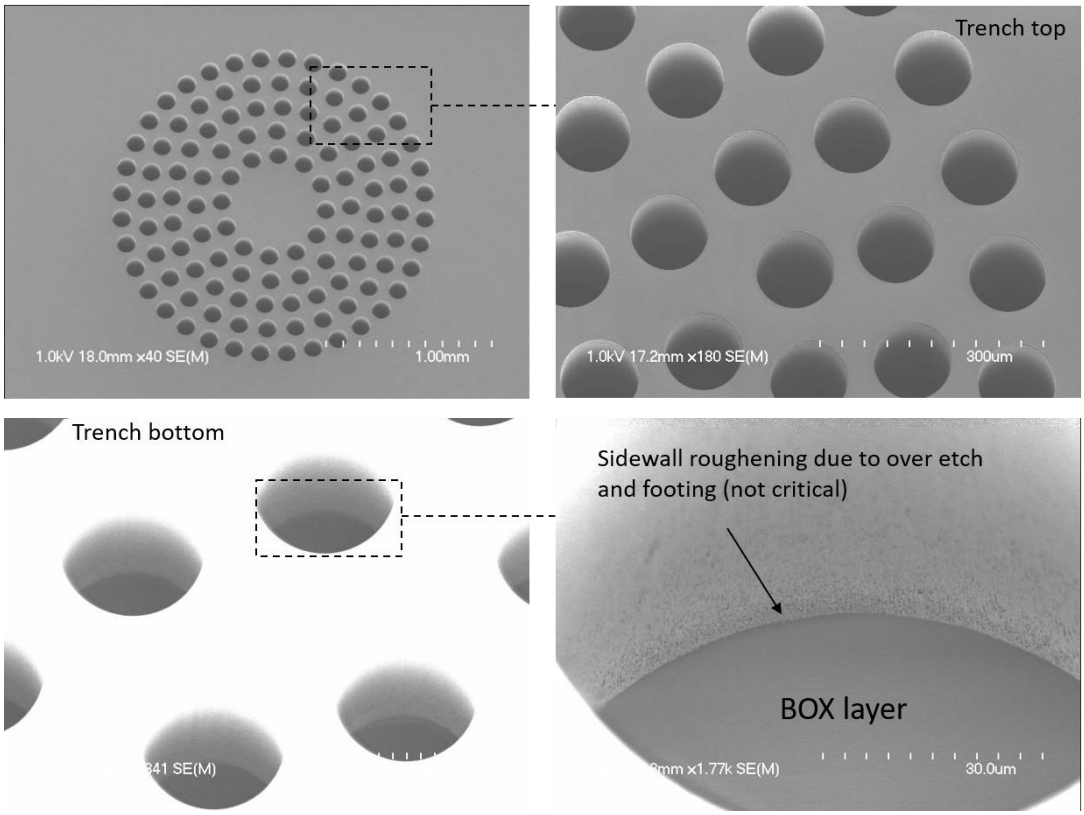

Figure 33 – Etching of backside holes through the handle layer symmetric to the mode shapes. It is important to note the rough bottom of the trench due to large footing and care must be taken that there are no striations or residues of silicon breaking off inside the trenches.

For this purpose, we use the STS Pegasus tool to basically etch “TSV-like” trenches through the handle layer. The recipe is given in Table 9. These backside holes as per the design are 100um in diameter and have an aspect ratio of about 4:1. While this aspect ratio is not hard in practice to etch for smaller thicknesses, the large 450um thickness of the handle layer and cleanliness of the trench makes it challenging. When using a high-power fast etching tool like STS Pegasus, the selectivity of the mask is very low. This means that we have to deposit a minimum of 4-5um of PECVD oxide at the back. The photoresist used to etch this oxide is retained during the actual trench etching, to provide more mask during the process. The etched backside holes are shown in Figure 33.

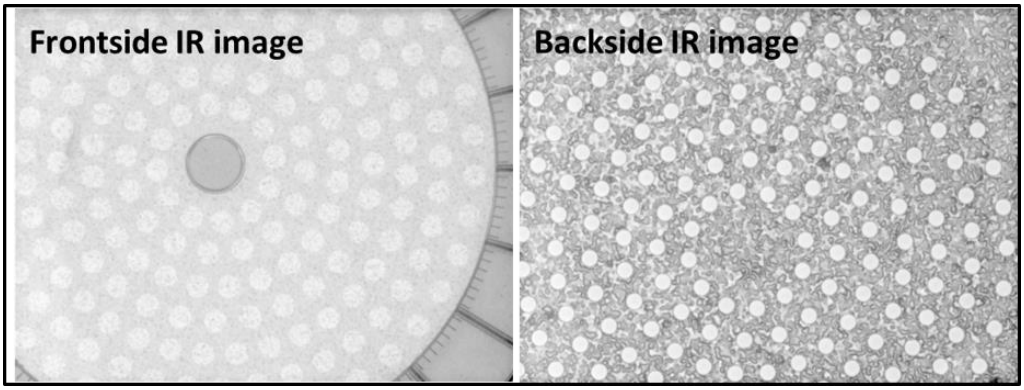

Figure 34 – IR images taken from a wafer with rough back side. The picture of the left shows that the back side holes are visible from the front side, but the front side features are not visible from the back as seen in the picture on the right. This is because of the rough back side which prevents IR transparency. Hence, the backside of the epipoly wafers must be ordered as polished, which is the case in Figure 33.

It is also worth mentioning, that the backside of the wafers should be smooth or polished and not rough. As shown in Figure 29, the thickness variation on the epipoly substrates has a large variation of about 5um across the wafer. Hence, having a smooth backside can allow IR transparency through the wafer, and makes it easier to check if the trenches have successfully reached the BOX layer during the trench etching step. The

initial wafer did not have a smooth back side, and made it hard to check the trench etching step. As a consequence, the trenches at the edge of the wafer were not fully etched, as also shown in Figure 29. An image of the rough backside holes is shown in Figure 34.

Table 9: Backside holes etching recipe in STS Pegasus

Parameter	**Value**	
	Etch	Passivation
Cycle time (s)	3.8	2
Throttle mode	Auto	Auto
Pressure (mT) (start, stop)	30, 25	15, 15
Gases (sccm)		
C_4F_8 (start, stop)	0, 0	150, 150
SF_6 (start, stop)	250, 300	0, 0
O_2 (start, stop)	10, 12	0, 0
13.56MHz Coil power (W)	2200	1900
LF Platen power (W) (start, stop)	80, 95	0, 0
Platen Chiller Temp (°)	-10	

3.4.5 Reduced-temperature HARPSS Process Flow

The process flow is shown in Figure 35. A 3μm layer of PECVD oxide is first deposited on the epi-poly wafer at 250°C, on both the front and back side of the wafer to nullify the stress of the film. Trenches are then etched on the wafer with a 45um substrate which define the resonator shape using the first mask (Figure 35a). A 300nm LPCVD oxide defining the capacitive gap is then deposited on the sidewalls at 725°C using TEOS, which is used as a substitute for high temperature oxidation (b). Alternately, a low temperature

oxidation can also be considered at 900°C. The trenches are then filled with LPCVD polysilicon which is conformally deposited on their sidewalls at 588°C. This polysilicon must be in-situ P/B doped, since diffusion and drive-in processes for polysilicon are generally at higher temperatures of 1050°C. The high temperature drive-in annealing generally reduces polysilicon stress. However, in this case, the polysilicon must be etched back to the surface of the oxide after every deposition to prevent the accumulation of too much LPCVD poly on the surface of the wafer, which may cause cracking due to stress (c).

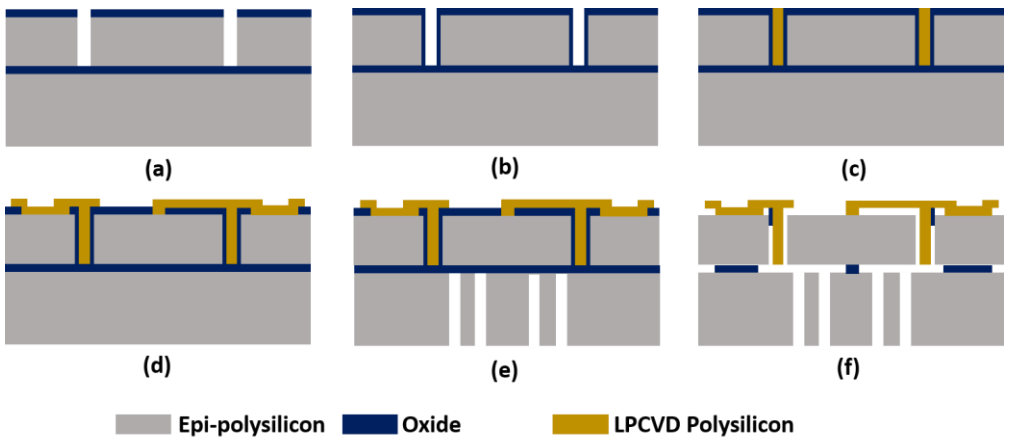

Figure 35 – The reduced-temperature HARPSS process for epi-poly disk resonators.

The top oxide is patterned on the surface over the electrodes and the top poly is then deposited with the same conditions as the vertical poly (d). Top poly is annealed at 850°C in N_2 after every deposition which reduces some stress from the top poly film. After this, the poly is etched from the unwanted trenches, defining the entire HARPSS electrode. A short oxidation is done at 850°C to oxidize any possible debris from the trenches. Finally, the backside holes are patterned at the back of the wafer and etched through to the BOX layer from the back side (e) and the devices are cleaned and released in 49% HF (f). The

fabricated SEM images of the poly disk are shown in Figure 36. It can be seen that the devices are not bent after release – the amount of bending can be measured with comparison to the electrode at the center and the edge of the disk. This is demonstrated in Figure 37.

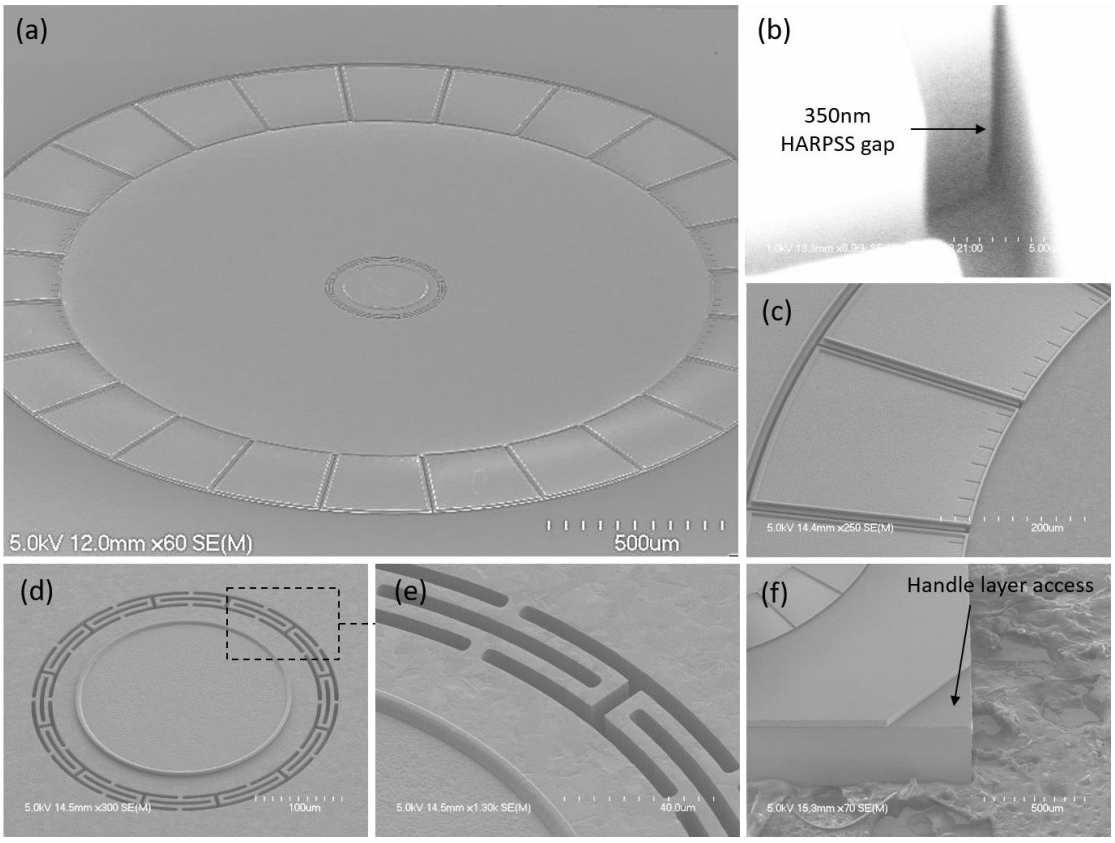

Figure 36 – SEM images of the fabricated epi-poly solid disk gyroscope; (a) picture of the entire disk and electrodes, (b) showing the HARPSS nano gap of 350nm at the bottom of the trench, (c) zoomed in view of electrodes, (d) and (e) showing zoomed in images of the center electrode and springs respectively, and (f) showing the corner of the die with access to the handle layer for biasing.

3.5 Epi-poly BAW Gyroscope Characterization and Testing

The fabricated epipoly disks were tested on a die-by-die basis on a PCB specifically designed in a way in which all the 24 electrodes could be wirebonded and switches were

present to use tuning and quadrature voltages. 1.88mm diameter disks were fabricated with a large post size of 250um which was achievable due to the decoupling tethers at the center of the disk. This large post size also enabled wire-bonding directly to the center of the disk without degrading the quality factor or having the need to use poly-plugs during fabrication. High *Q*s exceeding 1M were measured on the disks for n=3 mode shapes and the smallest mode split was 45Hz as shown in Figure 38. The as-fabricated gap size was about 340nm. This was due to the small difference in oxidation growth rate on polysilicon as compared to silicon which is hard to characterize perfectly.

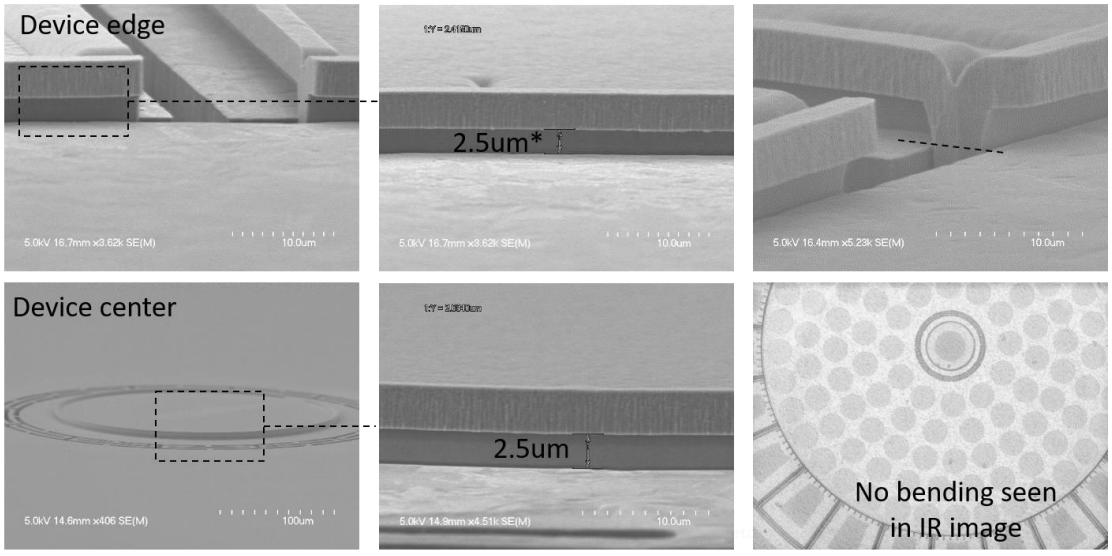

Figure 37 – SEM images of 2mm epi-poly disk as seen at a tilt of 10°. The device is seen to be well released in the IR image at the bottom right and it is not bent, as can be verified by measuring the distance between the electrodes and the disk at the center and edge of the disk.

The mode-matching of the peaks for the 45Hz mode-split device are shown below in Figure 38. It was seen that owing to a small mode split, only a small polarization voltage of 16V was required to mode-match the device completely, using a tuning voltage Vt = 15.2V and a quadrature voltage Vq = 14.32V. This is the first time in literature that a quality

factor exceeding 1M has been mode-matched for degenerate N=3 modes. Many devices on the wafer were tested, and the quality factor was consistently measured at ~1M. These measurements were taken on the network analyzer (Keysight E5080A). For gyroscope testing purposes, the device was then mounted on a height adjustment clamp on the rate table using an on-board vacuum chamber as shown in Figure 39. The circuit board consisting of discrete elements, was specifically designed to fit the height adjustment clamp, and also the on board vacuum chamber, in such a way that the vacuum tube faces the lease amount of resistance during rotation of the rate table.

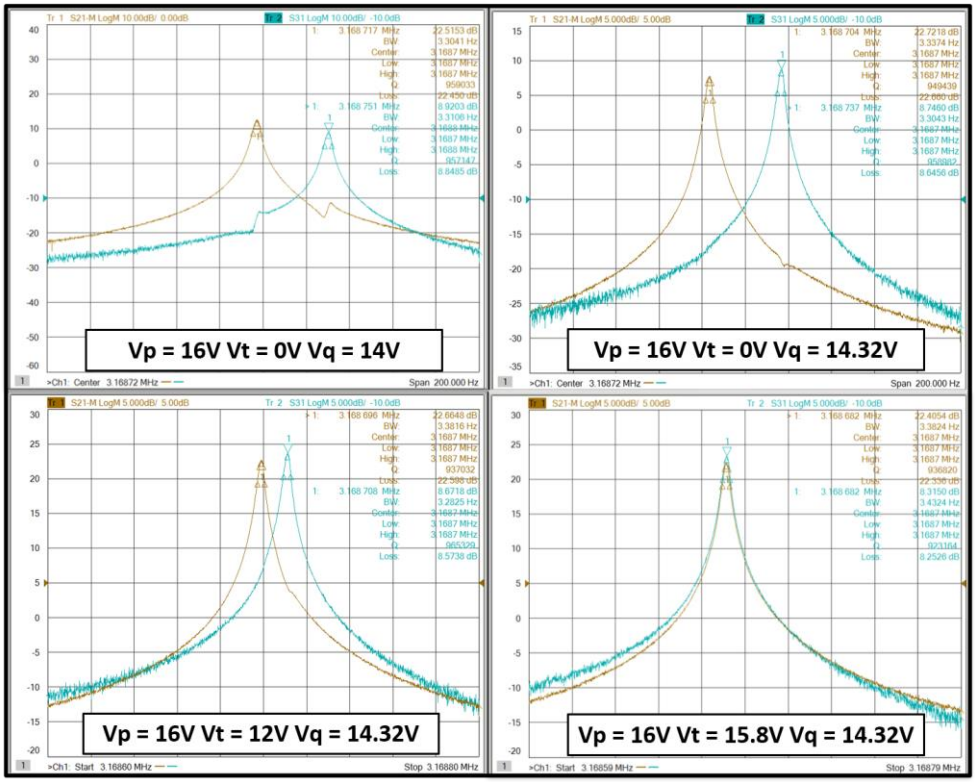

Figure 38 – Mode matching and quadrature cancellation of the degenerate modes of the epipoly disk for N=3 modes, for initial mode-split of 45Hz. The quality factor was in excess of 1M and it was the first time that a mode matched Q of 1M has been shown in literature.

The ADEV was measured using an HF2LI lock-in amplifier and the ARW was reported at 0.01 deg/√hr, which was coherent with the device design, as shown in Figure 40. However, it was seen that the bias instability of the device was particularly high at about 10 deg/hr. One of the reasons that this might have happened is suspect to the uncapped nature of the device, which was susceptible to temperature variations and drifts during the testing. Another reason for this might also be due to the fact that the vacuum pump had to be connected to the device board, which caused undulating vibrations to the PCB. The time domain response for various rate rotations are shown in Figure 41. The ZRO of this device, was extremely low < 1 deg/s, which is much lower than most SCS disk gyroscopes. However, this did not reflect in the ADEV plot in the bias drift of the epipoly design, one of the causes of which is the larger than expected frequency splits, which was one issue that was observed during the testing of these devices. This is investigated in the next section.

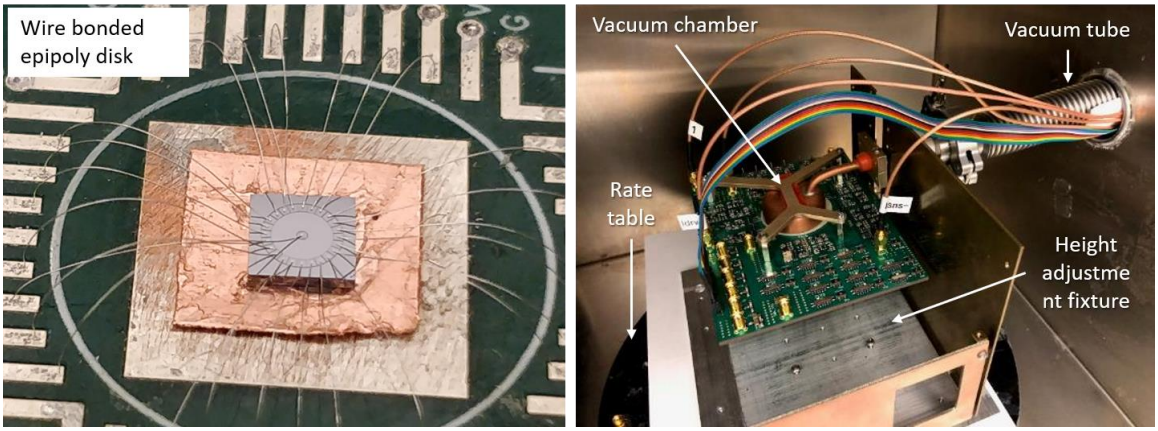

Figure 39 – A wire bonded epipoly disk gyroscope (left), and testing setup consisting of the PCB and the on-board vacuum chamber on the rate table (right).

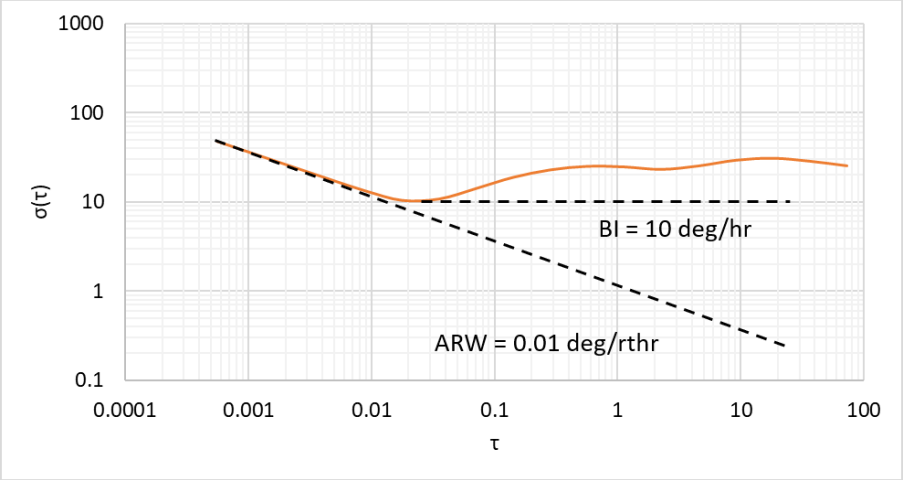

Figure 40 – Measured ADEV plot of the epipoly disk showing an ARW of 0.01 deg/√hr as designed and a bias of 10 deg/hr.

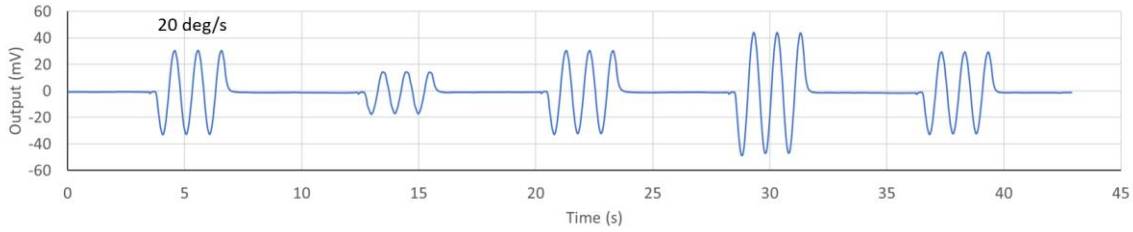

Figure 41 – The time domain response showing a scale factor of 7nA/dps, for different rotations with a ZRO < 1 deg/s.

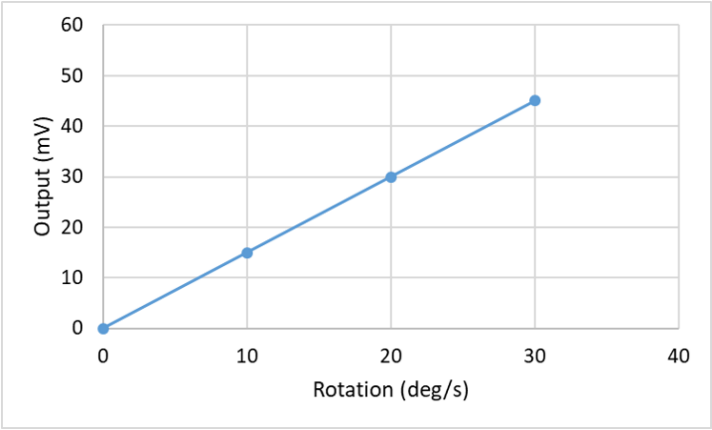

Figure 42 – Linear scale factor up to 30deg/s rotation. The device couldn't be tested for larger rotation because of the setup limitations in Figure 39, where the cables prevented the rate table from large rotations.

3.6 Two-mask Epipoly Disk Resonator Process

One of the drawbacks in the previous process during testing faced was the low yield on the gyroscopic designs in terms of frequency split. While many devices were measured with low frequency splits, most devices showed splits as large as 500Hz. This was unexpected, considering that the substrate should be isotropic in nature. However, to investigate this issue, a simple 2-mask process was run, consisting of the disk resonators formed by a single mask etch on the device layer and the second mask being the backside holes.

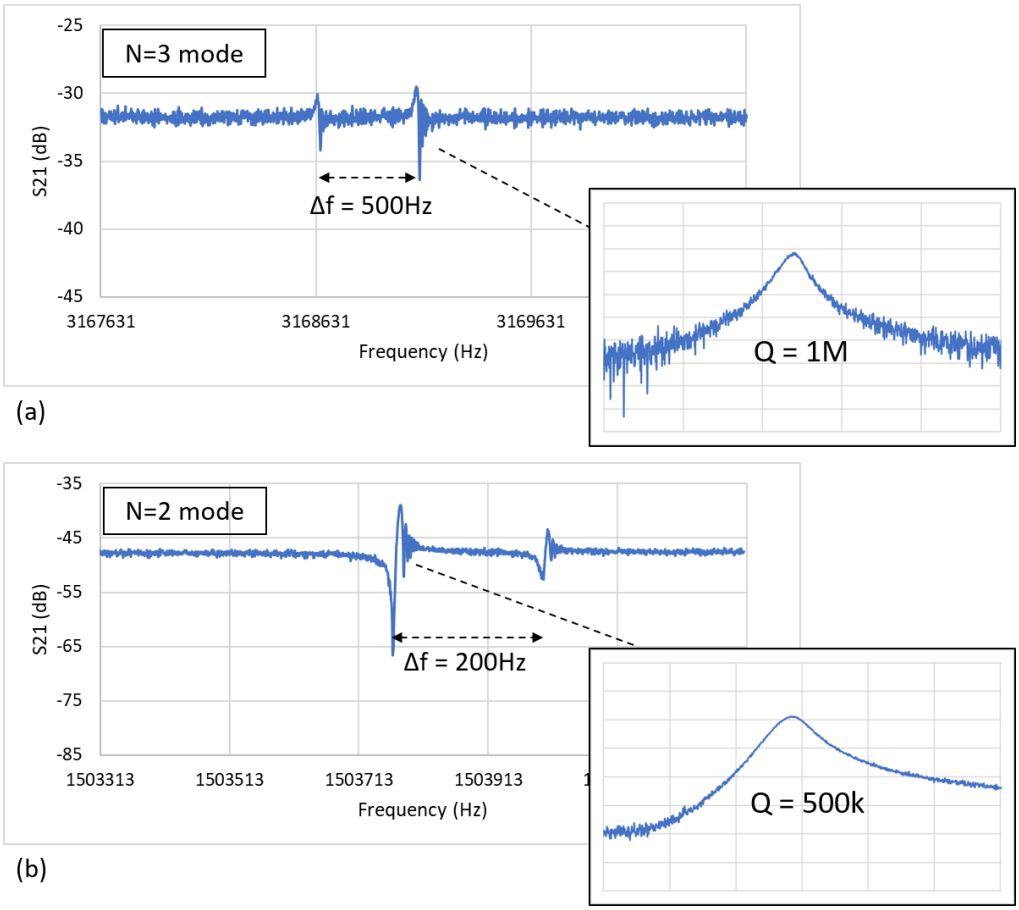

Figure 43 – Measured frequency splits for one of the devices each from two-mask process for (a) N=3 and (b) N=2 elliptical mode disk resonators.

The advantage of this process was that it would not be susceptible to even moderate temperatures, such as 588°C for polysilicon deposition, which was used in the reduced temperature HARPSS process. It was also expected to be devoid of any stress on the devices due to deposition of materials such as LPCVD polysilicon or TEOS, which might have induced a stress-related frequency split.

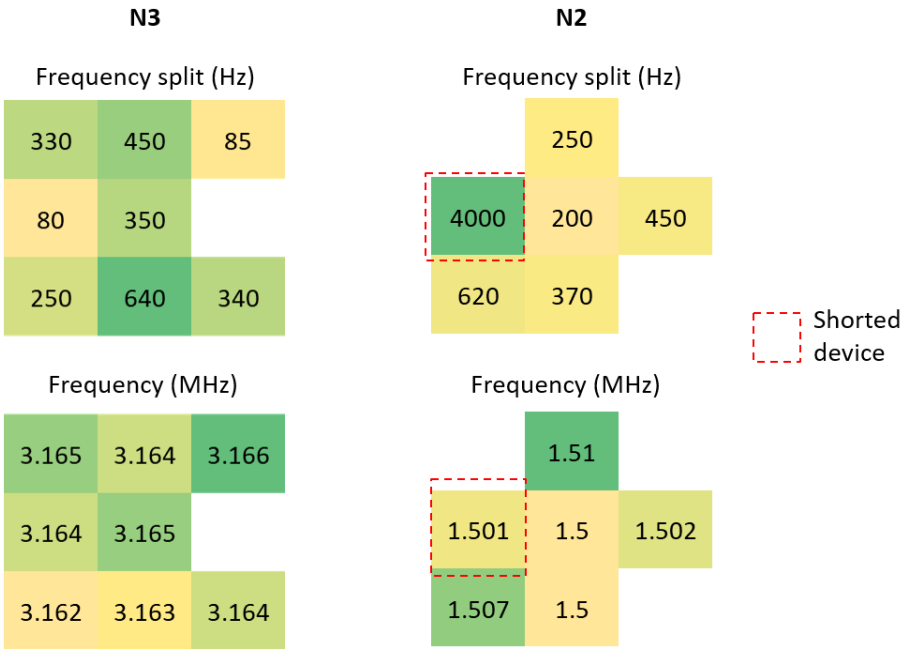

Figure 44 – Map of measured frequency splits of 9 adjacent devices for N=3 and N=2 modes. Blank spaces indicate devices that could not be measured because of fabrication asperities. We see that while the resonance frequency is consistent, the mode splits do not follow a trend within adjacent devices, thereby ruling out fabrication variations as a cause of large mode split.

However, as we tested these parts, we found that there are large frequency splits from even a simple two-mask process. The frequency splits from one of the devices for the N=3 and N=2 devices are shown in Figure 43. Also, it is important to note that the same *Q* of 1M was measured from the N=3 device as seen in the HARPSS process at the same frequency of 3.17MHz, while a *Q* of 500k was measured for the N=2 device at 1.5MHz.

Hence, despite showing similar results in terms of *Q* and frequency as in the HARPSS process, we still noticed a large frequency split. Therefore, it can be said that while the cause of the large split is not from the reduced temperature HARPSS, perhaps this was induced from the substrate itself, perhaps from irregular grain size, which could not be quantitively measured on these substrates. Also, it can be concluded that the frequency split was not from any kind of fabrication variation, since adjacent devices showed very different frequency splits, and was random in nature. Figure 44 shows a map of 9 adjacent devices tested for both N=3 and N=2 modes.

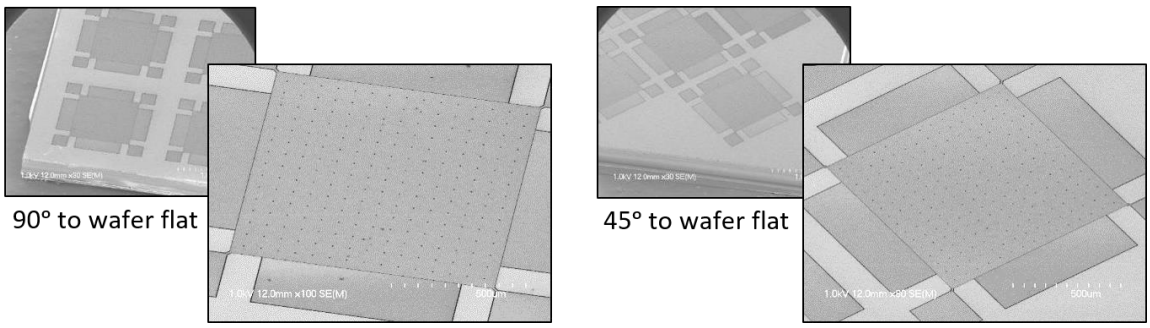

Figure 45 – SEM images of square Lame mode devices fabricated in the epipoly substrate for two different orientations (a) 90° and (b) 45° to the wafer flat.

For further verification of isotropy in these substrates, we also measured square Lame modes in two different orientations, 45° and 90° to the wafer flat. In a <100> SCS substrate, the frequencies of the devices in these two orientations would differ greatly from each other, whereas in an isotropic substrate such as epipoly, they should be the same. The square Lame modes had a side of length 1000um, and contained 4umx4um front side release holes, which result in a simulated resonance frequency of 3.7MHz for the device. Figure xx shows the SEM images of the two orientations of the square Lame mode devices. Measurements of 5 such devices showed an average frequency of 3.737MHz for the 90°

aligned devices and 3.732MHz for the 45° aligned ones. Simulation of the same devices in the <100> SCS substrate would have a resonance frequency of 3.3MHz for the devices aligned 45° to the wafer flat and 4.1MHz for the 90° alignment. Hence, as the measured frequencies for the devices in the epipoly substrate are very close to the simulated value, it verifies the isotropicity of the substrate. However, one noticeable aspect is that the frequencies in the 45° aligned devices are slightly higher than those in the 90° alignment, but this could be attributed to fabrication variations. The difference in the Q in each of these devices comes from the anchor loss, since some devices were measured from the edge of the die and some from the center.

Table 10: Measured frequency and Q in 5 epipoly square Lame mode devices in two orientations of 45° and 90° to the wafer flat.

Device number	90° Aligned		45° Aligned	
	Freq (MHz)	Q	Freq (MHz)	Q
1	3.738	93k	3.735	170k
2	3.738	156k	3.732	302k
3	3.737	312k	3.728	310k
4	3.737	323k	3.731	196k
5	3.736	240k	3.731	196k
Average	3.737	225k	3.732	259k

Therefore, while epipoly does show many advantages over SCS substrates for BAW disk resonators in terms of anchor loss and isolation, one unexpected feature in these substrates was the large mode split. While a high-performance gyroscope was measured in terms of *Q*, SF and ARW using this substrate and thereby proving its advantages, it was

seen that a lower ADEV could not be achieved. This was because of large mode splits, which reduced the decoupling between the modes. It was verified by the two-mask process that the deposition of other materials as well as moderate temperatures of 900°C were not the cause of the large mode splits. However, further investigation needs to be done on the development procedure of these substrates to find the cause of large mode splits.

3.7 Epipoly Dual-Axis In-Plane Accelerometers

Other than disk gyroscopes, in-plane accelerometers were also fabricated on the same platform. With the advent of emerging applications such as wearable health monitoring systems, Internet-of-Things (IoT), and indoor navigation, there is a rising need for high bandwidth, low noise multi-axis accelerometers with small form-factor. The dual-axis design uses the acceleration-induced translational motion of the proof mass with highly sensitive nano-gap transducers, which allows for high performance, matching single-axis designs while occupying a much smaller footprint.

3.7.1 Dual-axis accelerometer design

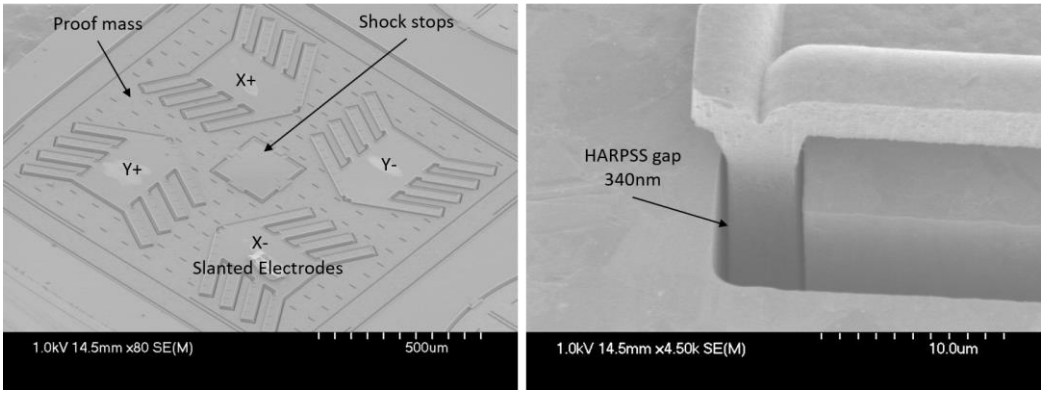

Figure 46 – SEM images of the dual-axis in-plane accelerometer showing the bird's eye view of the device (left) and the close up of the 340nm HARPSS gap in the slanted electrode (right).

The miniature translational dual-axis accelerometer can be used to overcome the tradeoff between performance and size. These devices show significant reduction in area as compared to single axis devices, while maintaining similar performance. Also, their translational motion results in higher effective mass, providing better signal-to-noise ratio compared to triaxial accelerometers while being operable in multiple axes. The accelerometer designed here uses 340nm capacitive gaps in a comb-finger configuration to achieve a high sensitivity and overcome tradeoff between operational bandwidth and noise performance.

Two pairs of differential electrodes – one for each axis, are housed within the proof mass to reduce the device size. The electrode fingers are placed in a sloped configuration to enable implementation of shock-stop structures. The proof mass is anchored at the edges within a decoupling frame which is anchored orthogonally to the device layer, thus enabling dual axis motion of the proof mass. The lengths of the tethers are designed to nearly match the resonant frequencies of the modes of operation corresponding to acceleration-induced translational motions. This configuration of tethers and decoupling frame ensures lower cross axis linear acceleration sensitivity, along with higher rejection of rotational motion. The small size (1.3mm x 1.3mm x 0.04mm) of the device also makes it an ideal choice for use in wearable health monitoring applications such as detection hand tremor, and joint angle measurements. The fabricated device is shown in Figure 46.

CHAPTER 4. DISTRIBUTED LAME MODE RESONATORS

Timing resonators are real-time clocks providing time-base references for electronics in automotive, industrial and consumer applications. Similar to tuning forks used for tuning musical instruments, a high-accuracy timing resonator with high robustness and temperature stability is an essential element for high-performance electronics. For this reason, a substantial part of timing resonator development has been based on quartz resonators owing to their superior temperature properties.

Silicon MEMS timing resonators, on the other hand, have drawn a great amount of attention as an alternative due to their small size, low cost, and more importantly integration compatibility with interface circuits on the same silicon substrate. However, they have had limited success in replacing their quartz counterparts in high-end applications; the bottleneck being the lack of temperature stability and frequency scalability with feasible motional impedance, especially at higher frequencies in the VHF range. In order to overcome the temperature variations, many methods are used [58], some of which include using compound materials [59] and using highly doped silicon substrates [14], [49]. Using compound materials usually involves complicated fabrications process, leading to higher cost and lower manufacturability. Therefore, the single-material solution is more attractive for reliable mass production. In silicon substrates, the doping changes the relationship of the elastic constants of silicon with respect to temperature, which in turn changes the temperature behavior of the device and improves the temperature stability for certain resonance modes. Specifically, resonators excited into Lamé mode resonance in a highly-doped silicon substrate present a frequency turnover point versus temperature.

Square Lamé mode resonators have been popularly used to attain high *f.Q* products owing to their low thermoelastic damping (TED) and ability to produce *Q*s over a million with frequencies in the range of 1-10 MHz [14]–[16], [49]. However, motional impedance requirements for low noise oscillator implementation and mode distortion due to anchoring restrict the minimum feasible size of the square Lamé mode resonators, limiting them to relatively low resonance frequencies that require up-converting frequency synthesizers with to additional phase noise and larger power consumption. Therefore, it is desirable to design a low motional resistance resonator at high frequencies with high-temperature frequency turnover point to overcome these drawbacks and qualify silicon resonators for high-end applications such as high-frequency IoT applications.

Different high frequency resonance modes have been investigated for silicon resonators, however they usually show large linear temperature coefficient of frequency (TCF) and suffer from large temperature instability [60] in addition to large motional impedance [61], [62]. Cross-sectional Lamé mode resonators have been demonstrated previously, eliminating the anchoring limits of square Lamé mode resonators and showing frequency turnover points at high frequencies [63]. However, such designs are sensitive to substrate thickness and have low robustness against process variations, affecting their manufacturability for mass production. Furthermore, their motional impedances can be high in the order of 100kΩ, adding difficulties in oscillator implementation.

In this work, we present a robust resonator design utilizing the in-plane shear nature of Lamé mode to create distributed resonance, which for the first time, enables high frequency, high-temperature TCF turnover point, low motional impedance, and high manufacturability at the same time. The wafer-level-packaged DLR allows us to achieve

high *f.Q* products at high frequencies (>50MHz) in a small footprint and without using getters, which makes it an ideal solution for high frequency, low-power temperature-stable applications. Table 11 briefly summarizes the enabling features of DLR as compared to other timing BAW resonators. Detailed design, simulation and experimental results are reported and discussion in the next section, followed by material and fabrication method information.

Table 11: Summary of features enabled by the distributed Lamé mode resonator as compared to other frequently used BAW resonators.

BAW resonator type	Low R_m (<10kΩ) at high freq. (>50MHz)	Robustness to thickness variation	High temp. turnover point (>90°C)
Square Lamé	✗	✓	✓
Cross sectional Lamé	✓	✗	✓
Width/length extensional (SiBAR)	✓	✓	✗
Distributed Lamé **(this work)**	✓	✓	✓

4.1 Distributed Lame Mode Concept

In typical silicon bulk acoustic wave resonators, primary (P-wave) or secondary vertical (SV-wave) elastic waves travelling through the resonator body reach the silicon-air interface and reflect back to form a combination of P and S waves, a phenomenon also called mode conversion. Now consider an SV-wave with amplitude B_1 incident at the edge of a resonator, which reflects back into a P-wave with amplitude A_2 and an SV-wave of amplitude B_2 as shown in Figure 47. The ratios of the amplitudes, which are solved using plane wave equations, can be given by [64]:

$$\frac{B_2}{B_1} = \frac{\sin 2\theta_1 \sin 2\theta_2 - k^2 \cos^2 2\theta_2}{\sin 2\theta_1 \sin 2\theta_2 + k^2 \cos^2 2\theta_2} \tag{2}$$

$$\frac{A_2}{B_1} = \frac{-2k^2 \sin 2\theta_2 \cos 2\theta_2}{\sin 2\theta_1 \sin 2\theta_2 + k^2 \cos^2 2\theta_2} \tag{3}$$

Here, θ_1 is the angle of reflection of the P-wave and θ_2 is the angle of incidence and reflection of the SV-waves B_1 and B_2 respectively, and k is the ratio of the wavenumbers γ_2/γ_1. From the equations (2) and (3), we can calculate that for the special case wherein θ_2 = 45°, we get $A_2/B_1 = 0$ and $B_2/B_1 = 1$. From these two ratios, we can see that for an SV-wave incident at 45°, the resulting reflection is only an SV-wave. This pure SV-wave nature of Lamé mode indicates that a series of Lamé modes can result from a propagating train of S-waves at 45°. A few such modes are shown in figure 1. These modes retain the thermal and mechanical properties of a square Lame mode.

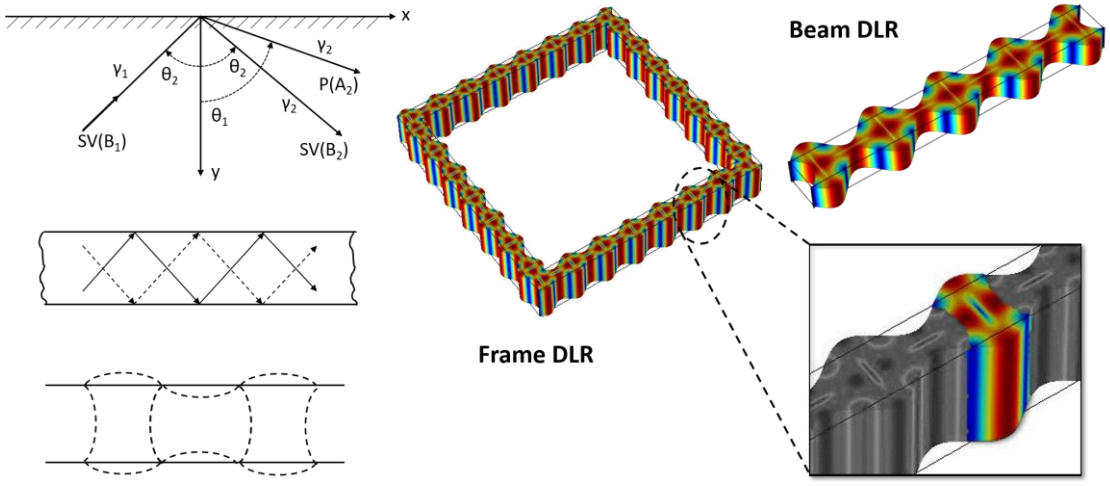

Figure 47 – Animation of a propagating train of Lamé modes in the shape of frame and beam structures and (inset) highlighted deformation of one distributed element.

Using the above concept, it is possible to actuate a series of Lamé modes "distributed" in a rectangular beam or a frame with a uniform width of a single square Lamé mode (Figure 47). Such designs, known as distributed Lamé resonators (DLR) were fabricated on both single- and poly-crystalline silicon SOI wafers, the process flow of which is explained in the next section. The distributed configuration, especially the frame structure, provides more design freedom in performance scaling. To further explain this, we have to consider the frequency *f* of square Lamé mode resonator aligned to the <100> direction is given by [65]:

$$f = \frac{1}{\sqrt{2}.W}.\sqrt{\frac{c_{11}-c_{12}}{2\rho}} \tag{4}$$

Here, *W* is the width of the resonator, c_{11} and c_{12} are primary elastic constants, and ρ is the density of silicon. We can easily see that in order to get high operational frequency, the width *W* of the square device needs to be extremely small, which significantly sacrifices the transduction efficiency for oscillator applications. The motional impedance R_m of a square Lamé mode with a pair of actuation and readout electrodes is given by [66]:

$$R_m = \frac{2\pi\gamma M f g^4}{Q\varepsilon_0^2 W^2 t^2 V_p^2} \propto \frac{\rho W^2 t f g^4}{Q V_p^2 W^2 t} \propto \frac{f g^4}{Q V_p^2} \tag{5}$$

where γ is the mode-shape related transduction coupling ratio, *M* is the effective mass of the resonator, *Q* is the quality factor, *t* is the device thickness, *g* is the transduction gap size, and V_p is the polarization voltage. For a square Lamé mode to be designed at higher frequencies, we see that the width *W* of the resonator would have to be small which relates

to a loss of transduction area, thereby making the motional impedance increasing proportionally with the frequency. In addition, for properly designed Lamé mode resonator, the *Q* is close to the Akheizer limit of silicon, which decreases at high frequencies, further increasing R_m. Consequently, the rapid increase in motional impedance prevents one from up-scaling the operational frequency, which highly limits the application of a square Lamé mode resonator.

In DLRs, length can be extended to a much longer multiple of the width. This does not change the frequency of the device, since the frequency is governed only by the width *W* of the resonator. However, doing this effectively increases the transduction area by allowing a discontinuous electrode arrangement. While the effective mass scales linearly with the number of unit square Lamé mode cells, the combined effect of increased actuation and readout transduction areas scales quadratically as the length of the resonator and number of unit cells increase, thereby improving R_m and minimizing the insertion loss as compared to a square Lamé mode. For a DLR with 2*N* unit cells and *N* electrode-pair-digits (one electrode-pair-digit for every alternate unit cell), the motional impedance is given by:

$$R_m = \frac{2\pi\gamma M f g^4}{Q\varepsilon_0^2 N^2 W^2 t^2 V_p^2} \propto \frac{2N\rho W^2 t f g^4}{N^2 Q V_p^2 W^2 t} \propto \frac{2}{N}\frac{f g^4}{Q V_p^2} \tag{6}$$

Comparing Eqn. (5) and (6) we can see, the increase in frequency and drop in *Q* can be compensated by extending the resonator length and increasing the number of electrode-digits and unit square Lamé mode cells. This shows that the decoupling of width and length offers design freedom to scale the frequency without compromising transduction efficiency; wherein the DLR shows a clear advantage over square Lamé mode resonators.

4.2 Salient Features of Distributed Lame Mode Resonators

4.2.1 Frequency Scaling of DLR

To verify frequency scalability and the motional impedance reduction of DLR designs, various DLRs of different widths *W* were fabricated in the beam (BDLR) as well as the frame (FDLR) configuration. The beam or frame width determines the resonator frequency, matching the frequency of a square Lamé resonator with the same width. The various parameters measured for different types of resonators are highlighted in Table 12. Figure 48 shows the comparison of high *f.Q* product in-plane Lamé mode silicon resonators in literature [14], [16], [54], [46]–[53] with the resonators fabricated in this work. With the distributed design, the three DLRs with narrow beam width successfully demonstrated high frequencies beyond the reach of any other in-plane Lamé mode designs, while maintaining a high *f.Q* product close to the Akhiezer limit of silicon. More importantly, low motional impedances are achieved on these DLRs despite having much higher frequencies.

Table 12: Various beam and frame DLRs of different dimensions, showing the features enabled using this design, with high frequency, low motional impedance and high Q.

Design	BDLR1	BDLR2	BDLR3	FDLR1	FDLR2	Epi-poly FDLR
Frequency (MHz)	41	51	95	167	51	58
Width (μm)	80	65	35	20	65	65
Length (μm)	720	845	525	300x4	845x4	845x4
Thickness (μm)	60 +/-1	40 +/- 0.5	40 +/- 0.5	40 +/-0.5	40 +/- 0.5	45 +/- 2.5
Gap size (nm)	300	270	270	180	270	340
Electrode-pairs	4	7	8	22	24	24

Q-factor (k)	123	148	94	72	250	86
R_m (kΩ)	80	6.1	19	6.2	0.56	9
Doping level (cm^{-3})	5-7x10^{19}	1-2x10^{18}	1-2x10^{18}	1-2x10^{18}	1-2x10^{18}	3-5x10^{17}

For example, in the FDLR2 version of the resonators, polarization voltage up to 30V was applied to the resonator body to characterize its motional impedance with a network analyzer (Keysight E5080A). A *Q*-factor loading effect was observe as the polarization voltage increase, which is usually seen for low motional impedance resonators[67]. Measurements with polarization voltage up to 5V show an unloaded *Q* ~254k, whereas a loaded *Q* ~135k was observed at 30V. For the loaded Q-factor, we have the following equation [67]:

$$Q_{loaded} = Q_{unloaded} \times \frac{R_m}{R_{total}} \tag{7}$$

where $R_{total} = R_m + R_{load}$, and R_{load} is the parasitic resistance in series with the motional resistance R_m of the device. Based on the insertion loss, the total impedance at 30V is calculated to be 1.06kΩ. From equation (7) and measured *Q*-factors, we can calculate the motional impedance of this device at 30V to be as low as 563Ω, as shown in Figure 49. The parasitic resistance R_{load} includes the two 50Ω terminations of the network analyzer, the physical resistance of the resonator body estimated to be 300Ω - 400Ω and small contributions from the through cap vias resistance between 20Ω - 40Ω. The existence of body resistance contribution is because for the DLR, the displacement at either side of the electrodes is in phase, as the resonator deforms periodically, net charges will flow in and out the DC port through the body of the resonator, which results in the resistance of the

resonator body loading the *Q* [67], [68]. This body resistance caused *Q* loading effect has also been shown previously for width extensional SiBAR [69] and IBAR devices [70]. The simulated values of the *Q*-factors due to different dissipation mechanisms for this design are shown in Table 13. With the Lamé mode having very low thermoelastic damping [71], it is seen that due to the high-frequency of operation of DLR, the *Q*-factor is limited by a combination of the Akhiezer limit in silicon and the anchor loss. While the Q_{ANC} in current designs was ~1M with 4μm-wide tethers, simulations show that a modified fabrication process with smaller critical dimension limit will enable Q_{ANC} of 80-100M with narrower or T-shaped tether designs. In addition, incorporating other substrate-decoupling mechanisms such as reflector structures or phononic crystal structures [72]–[74] may further improve Q_{ANC}. The Q_{TOT} based on simulations and assumed Akhiezer limit of 2.3×10^{13} was calculated to be around 300k. The measured *Q* of 250k is slightly lower possibly due to a lower than expected Akhiezer limit [75] or larger than simulated anchor losses caused by different device mounting conditions.

A further comparison of reduced motional impedance by frequency scaling can be made from the BDLR3 and FDLR2, which have the same width of 65um and thereby the same frequency which is approximately 50.7MHz as fabricated. With a polarization voltage of 25V, the loaded *Q*-factor of both devices are similar (~150k) and the motional impedance are measured to be 1.48kΩ for the frame DLR and 6.1kΩ (~4x higher) for the beam DLR, reflecting the 4x more distribution length and number of unit square Lamé mode cells in the frame DLR.

Table 13: Simulated values of Q-factors for FDLR2 design. Q_{AKH} calculated based on simulated frequency and a theoretical Akhiezer f.Q product limit of 2.3×10^{13}. These devices show a combination of Q_{ANC} and Q_{AKH} in the total Q-factor. While the Q_{ANC} in this current design was ~1M owing to fabrication limitations, simulations show that a modified fabrication process with smaller critical dimension limit will enable Q_{ANC} of 80-100M with narrower or T-shaped tether designs.

Simulated *Q*-factor for FDLR2	Value
Q_{TED}	68M
Q_{SFD}	3B (1Torr)
Q_{ANC}	1M
Q_{AKH}	450k
Q_{TOT} *(theoretical)*	300k

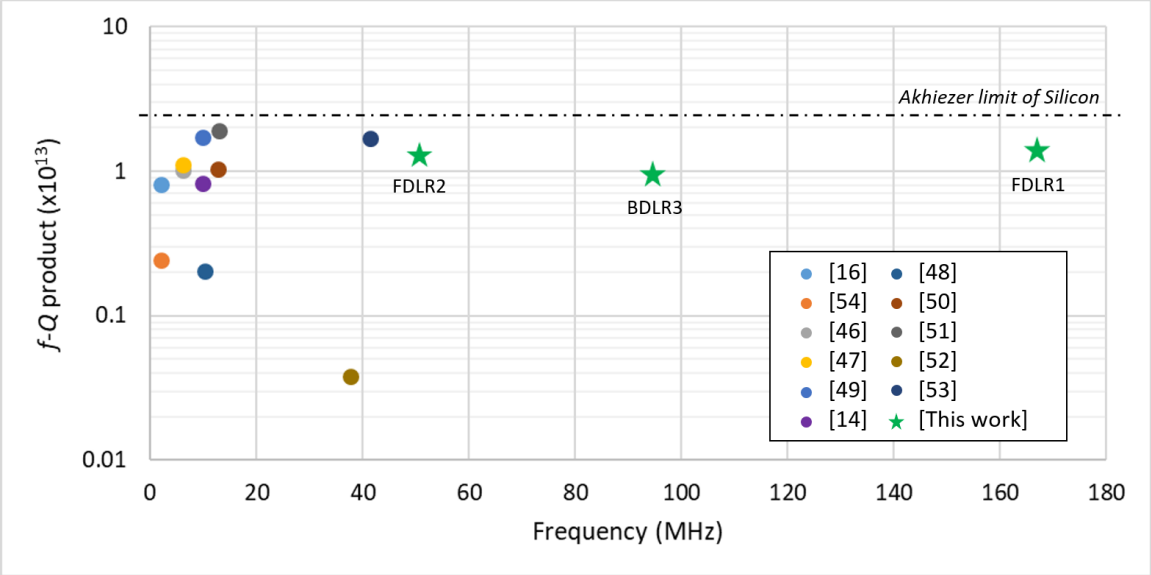

Figure 48 - Comparison of high f.Q in-plane square Lamé modes in literature with the devices designed in this work; a clear distinction can be made in terms of frequency, showing that the DLRs allow us to implement resonators at much higher frequencies than the square Lamé modes, with comparable f.Q products and a low motional resistance.

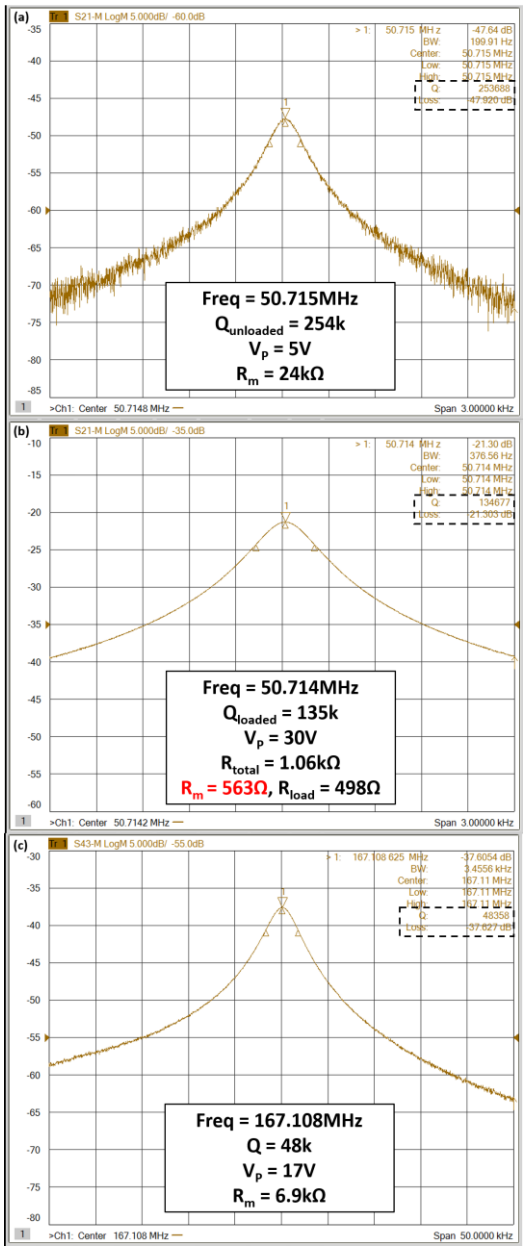

Figure 49 - Screenshots of the measured frequency response on a network analyzer of the same FDLR2 device showing the Q loading due to its parasitic resistance because of low motional impedance for (a) low and (b) high polarization voltages. (c) FDLR1 measured at 167.1MHz, showing a high Q of 48k with a low motional impedance.

Further using this concept, we were able to demonstrate a FDLR1 with a frequency as high as 167MHz with a device width of 20μm on a 40μm thick substrate [26], whose motional impedance is only 6.2kΩ with a relatively low polarization voltage of 17V which

can be generated by typical CMOS circuits. A thick square Lamé mode resonator with such small width and high frequency exceeds the capability of current micro-machining technology for reliable mass fabrication, needless to say the motional impedance of a square device with such dimensions would exceed 100kΩ, making it improbable for low-noise oscillator implementation. This clearly highlights the advantage that a DLR offers as compared to square Lamé mode resonators. When being used to build oscillators, this low motional impedance and insertion loss will reduce the gain requirement on the amplifier circuits, making it more practical to achieve high oscillation frequencies. Furthermore, for the 167MHz resonator, an unloaded *Q* of 77k was measured at 3.5V, corresponding to an *f.Q* product of 1.3×10^{13}, which is amongst the highest *f.Q* products measured in silicon.

4.2.2 Frequency Turnover Point on Highly-Doped Devices

An important feature of the square Lamé mode is the strong doping dependency of its frequency temperature behavior. A square Lamé mode on a highly n-doped substrate has been known to show a turnover point at high temperatures (>100°C) for doping level above $4 \times 10^{19} cm^{-3}$ [76]. At the turnover point, the slope of frequency vs temperature curve becomes zero. A high-temperature turnover point is important for highly stable oscillator design as it allows for ovenization of the resonator at its turnover temperature to improve frequency stability over the entire temperature range of interest. This important TCF property is maintained for the distributed Lamé mode due to the same nature of wave propagation and energy distribution as a square Lamé mode resonator. The turnover point however, is sensitive to doping variation.

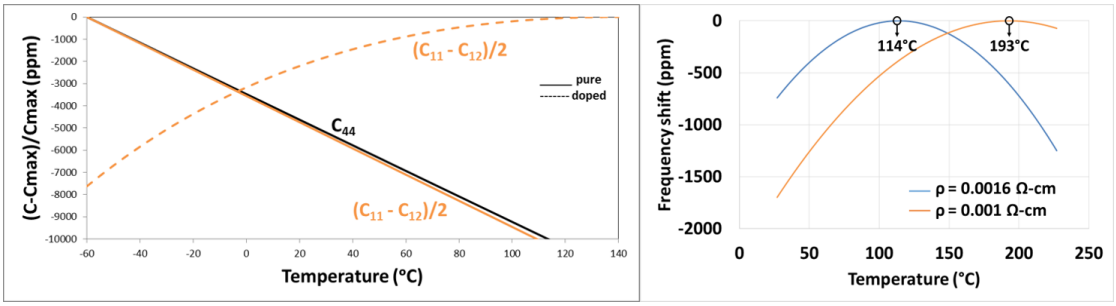

Figure 50 – Simulated curves for elastic constants of silicon for Lame mode resonators in the <100> and <110> directions for N-doping (left), and the corresponding temperature-frequency turnover points for two different doping concentrations of SCS (right).

To verify this, the temperature-frequency relationship of the DLR fabricated on highly-doped wafers was characterized in a temperature chamber. This was done on the BDLR1 devices shown in Table 12. A quadratic TCF profile is observed on various BDLR1 devices as expected, with the maximum turnover point measured to be at 170°C and a minimum turnover point of 95°C as shown in Figure 51, which agrees well with the simulated value for the doping range considering the doping variation across wafers. The TCF around the turnover point is close to zero, therefore ovenizing the device to maintain its temperature at the turnover point will allow one to build an extremely frequency-stable oscillator that are suitable for high-frequency timing applications over a wide range of environment temperature [77].

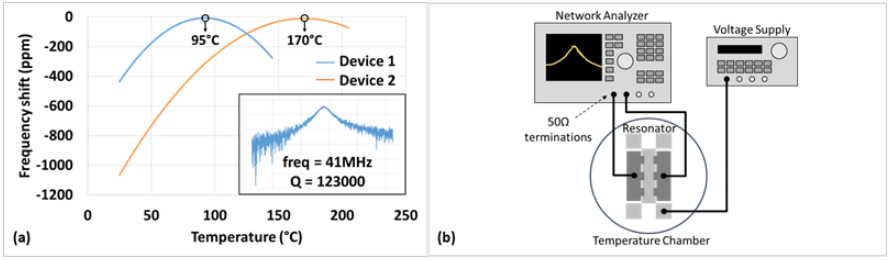

Figure 51 – (a) Measured turnover points at 95°C and 170°C for two beam DLR devices having a doping concentration variation of 5 to 7x10^{19}cm^{-3}and Q of 123k is

measured at 41MHz for the beam DLR1 design (a, inset), where the TCF at the two turnover points is zero; (b) measurement setup of the DLR using a temperature chamber and network analyzer for frequency read-out.

The turnover points can be derived from literature using various formulas that govern the equations of the elastic constants and deformation potentials of the semiconductor. The electrons of a many valley semiconductor tend to redistribute themselves in available energy levels so that the total free energy G is minimized [78]. Furthermore, the elastic constants in a semiconductor are said to be strain derivatives of electron concentration [79]:

$$\partial c_{ij} = \frac{1}{V_0} \cdot \frac{\partial^2 G}{\partial S_i \partial S_j} \tag{8}$$

Here, c_{ij} are the elastic constants in directions ij in a cubic crystal and ∂Si and ∂Sj determine the changes in strain in the *i* and *j* directions respectively. On addition of doping impurities in the semiconductor, the strains in the *i* and *j* directions change. This also changes ∂cij, in order to keep the Gibbs' free energy G minimum. The deformation potential model states that the strain shifts a band in energy without changing shape or other parameters. This shift in band energy, changes the Fermi energy level by a few hundredths of a volt. However, by adding doping impurities, we can cause changes in the strain which is described by the deformation potential, and this shifts the band energy by many volts. This changes the elastic constants as a function of temperature, as shown below.

In the case of n-doped Si, the contribution of the electrons to elastic coefficients is given as [80]:

$$\partial c11 = -\frac{2}{9} N \frac{Eu^2}{Ef} X \tag{9}$$

$$\partial c12 = \frac{1}{9} N \frac{Eu^2}{Ef} X \tag{10}$$

$$\partial c44 = 0 \tag{11}$$

Here, X=η.($F'_{(1/2)}$ (η))/($F_{(1/2)}$(η)) with η=Ef/kT and Ef = 25meV. Eu is the deformation potential. Using the value of Ef and k, η can be recalculated as 290.112/T. $F_{(1/2)}$(η) and $F'_{(1/2)}$(η) were calculated for all values of T from look up tables for Fermi-Dirac integrals. Also, we have the relation between Fermi integrals given as [81]:

$$F'_{\frac{1}{2}}(\eta) = \frac{1}{2} . F_{-\frac{1}{2}}(\eta) \tag{12}$$

Using the above equations, we can calculate the values for ∂c_{ij}. The total change in elastic constants will therefore be given as $c_{ij}(T)$=$c_{(ij,pure)}(T)$+$\partial c_{ij}(T)$, where $c_{(ij,pure)}(T)$ is the change of elastic constants of pure (undoped) Si with temperature. For a Lame mode in the <100> direction, the equation for frequency depends on c11 and c12 as given by equations (9) and (10). For the <110> direction, the frequency of Lame mode is only dependent on c44, and from equation (11) we see that c44 doesn't change with respect to temperature. Therefore, in order to get a turnover point for n-doped Lame modes, it is essential for the designs to be in the <100> direction. This is shown in Figure 50. Also, various turnover points for different doping concentrations have been plotted in Figure 50. The MATLAB code for calculation of these values is given in Appendix A.

4.2.3 Substrate Sensitivity and Compatibility

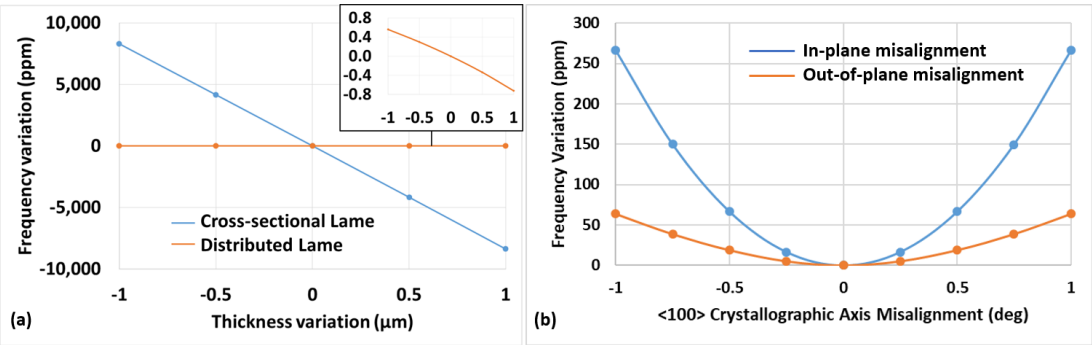

Figure 52 - Simulated (a) thickness variation of +/-1um shows a large frequency variation of +/-8200ppm for cross-sectional Lamé mode as compared to DLR which shows +/-0.6ppm; (b) variations of +/-266ppm and +/-63ppm for IP and OOP variations respectively in the <100> crystallographic axis.

Another advantage of the DLR in terms of fabrication compatibility is its high robustness over device thickness variations. One of the major challenges in fabrication of devices on SOI wafers is the thickness variations on the device layer across the wafer. At very high doping levels close to the solid solubility of the dopant species in silicon, the thickness variation across the wafer can range from +/-1µm to +/-5µm for commercial SOI wafers.

Previous work [63] has shown incorporating the Lamé mode in a cross-sectional orientation, enables a high frequency device to be used as a Lamé mode with increased transduction area. However, due to the thickness dependency of the device, the fabrication of such a device becomes difficult and not reliable due to the effect of thickness variation. In contrast, since the DLR is formed by in-plane S-wave reflections, the thickness dependency is eliminated, and better control of the mode shape is enabled even in the presence of large thickness variations as shown in simulated results across thickness

variations in Figure 52. While a comparable cross-sectional Lamé mode resonator showing ~1.6% frequency variation, the DLR, due to its in-plane nature, has only a frequency variation of +/-0.6ppm over +/-1µm thickness variation.

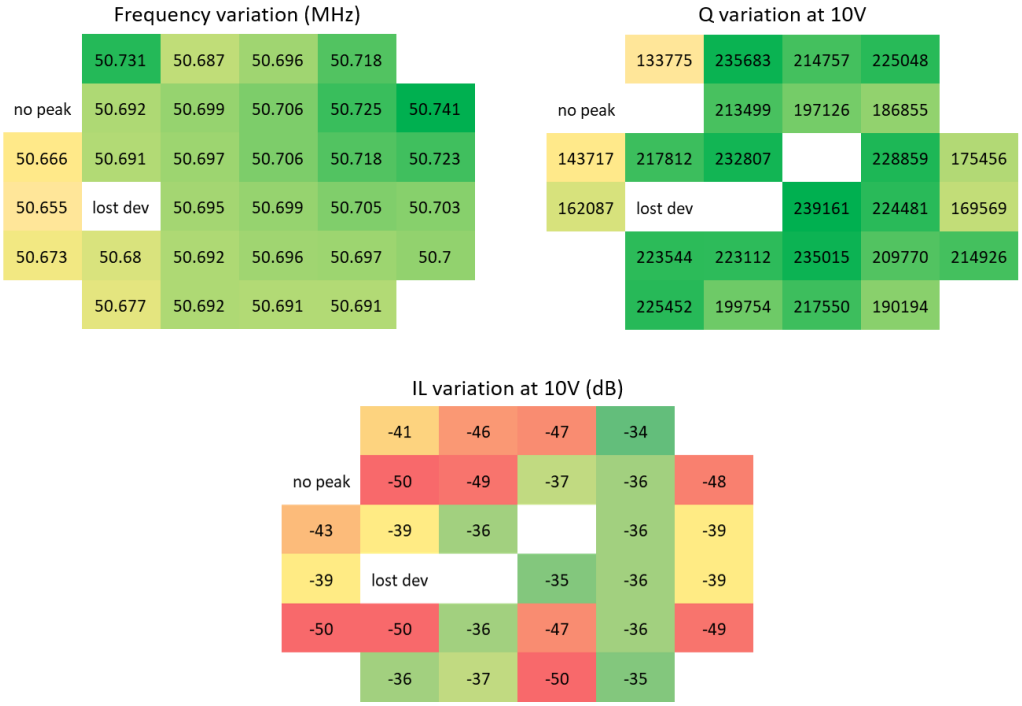

Figure 53 – Frequency, Q and insertion loss variation across wafer 1. This wafer shows a Δf/f of 1700ppm across the whole wafer, but a Δf/f of only 800ppm if edge dies are excluded. The insertion loss is low on some devices, because not all the electrodes of the frame device were properly bonded to the capping wafer, reducing the transduction area of the device.

Another common variation in single-crystal silicon (SCS) substrate is the crystallographic misalignment errors, which were simulated and shown in Fig. 5. A frequency variation of about 266ppm was seen for the FDLR2 design for an in-plane crystallographic variation of +/-1°, and a 63ppm variation for an out-of-plane variation of +/-1°, which is typical range of errors that can be seen in commercially available SOI wafers. While these frequency variations are tolerable for resonators in SCS substrates,

they can be completely negated by using an isotropic substrate such as epipoly-silicon substrate. This highlights one of the advantages of using epipoly as an alternate substrate to fabricate this device, in which crystallographic misalignment errors do not exist due to its isotropic nature. A frame DLR design was successfully demonstrated on an 45µm epitaxially-grown polysilicon SOI with a thickness variation of +/-2.5µm. Measurements show a frequency of 58MHz and *Q* of 86k, with a low motional impedance of 9kΩ, verifying the compatibility of DLR design with different substrates even with large thickness variations. An epi-poly substrate will also benefit the implementation of high-performance axial symmetric gyroscopes, showing a path towards fully integrated single-substrate timing and inertial measurement unit (TIMU) [56].

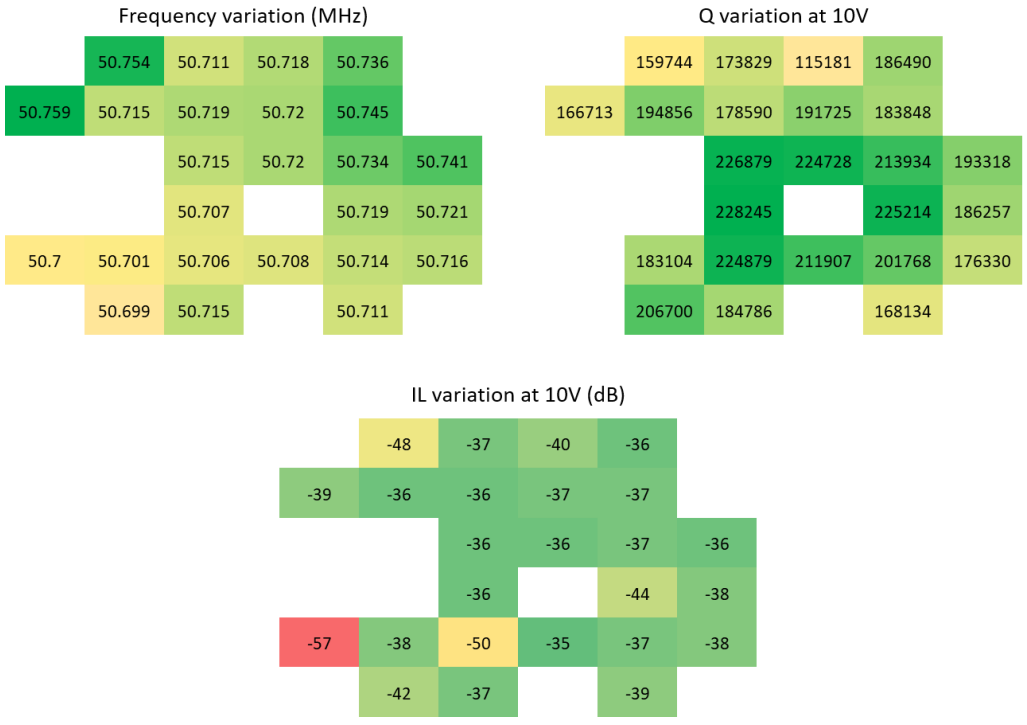

Figure 54 – Frequency, Q and insertion loss variation across wafer 2. This wafer shows a Δf/f of 1200ppm across the whole wafer, but a Δf/f of only 800ppm if edge dies are excluded. Consistent bonding on this wafer showed a fairly uniform distribution of insertion loss, Q and smaller frequency split as compared to wafer 1.

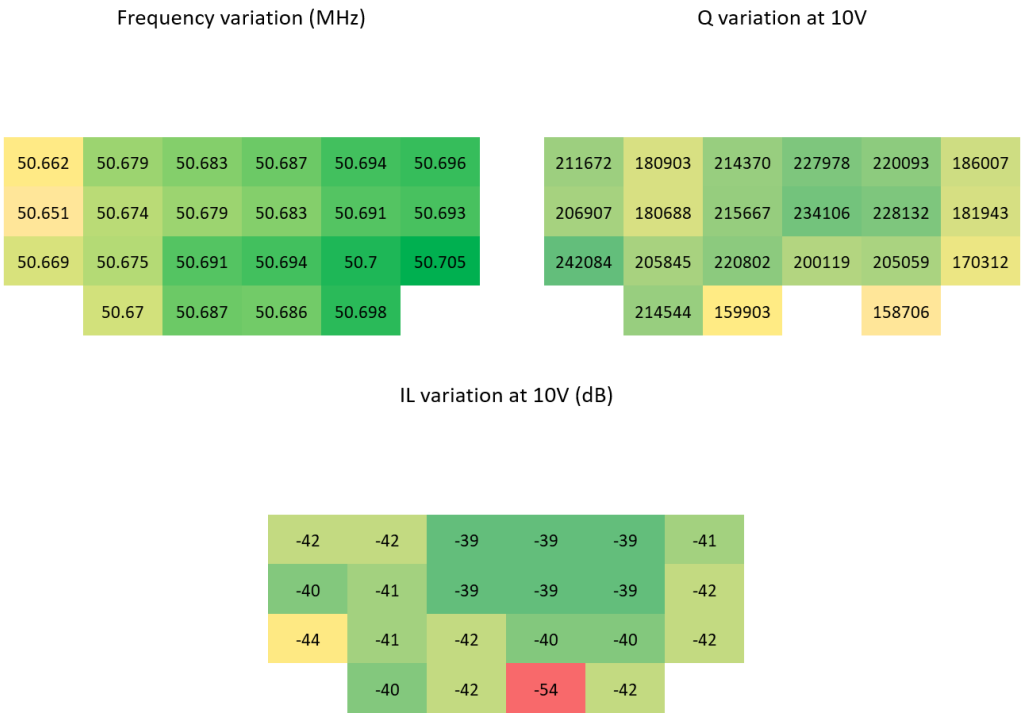

Figure 55 – Frequency, Q and insertion loss variation across wafer 3, which was the thinned down wafer to 450um. While the top two rows were not tested. this wafer shows a Δf/f of 1000ppm across the whole wafer, but a Δf/f of only 500ppm if edge dies are excluded. This wafer had the smallest mode split across the wafer even after the thinning down process, which shows high robustness in the wafer-level package and also the resonator design.

4.2.4 Manufacturability and Reliability

The WLP HARPSS process [4], [55], [56] is an advanced fabrication platform commonly used for creating high-aspect-ratio sub-micron gap devices operating in low-pressure environments. Encapsulated DLR die are fabricated using the HARPSS process and the frequencies and *Q*-factors are measured with good consistency as shown in Figure 56. Devices across the wafer were tested on 3 different wafers. Results show a within wafer frequency variation of about 800ppm at 50.7MHz, and an across wafers mean frequency variation of 1000ppm. *Q*-factors were measured to be between 200k to 253k with higher *Q*s measured close to the center of the wafer, which is possibly due to a process variation

induced anchor loss difference. In future designs, adding substrate decoupling structures such as phononic crystals to the tether or anchor designs may significantly reduce anchor loss, leaving the DLR *Q*s limited mostly by the Akhiezer loss in silicon.

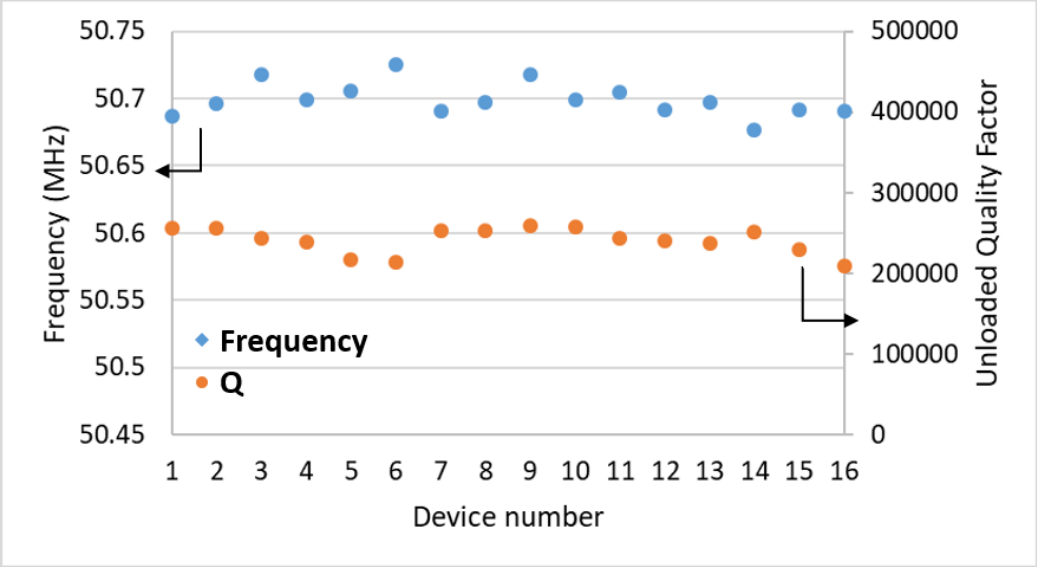

Figure 56 - Measured frequencies and Q-factors of 16 WLP die of the FDLR2 design, showing repeatability in yield from device fabrication with as fabricated Δf/f spread of 800ppm within wafer 1; the highest Q-factor achieved was 253k from devices close to the center of the wafer; Q-factor varies between 200k-253k because of fabrication variations in trench width causing resonator tether widths to change slightly.

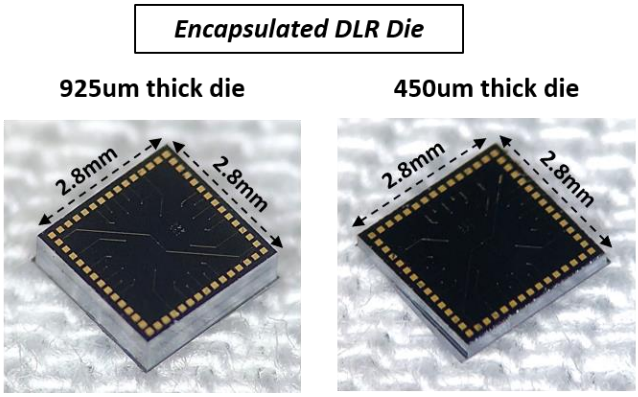

Figure 57 - Optical images of the 925µm and grinded 450µm thick WLP dies.

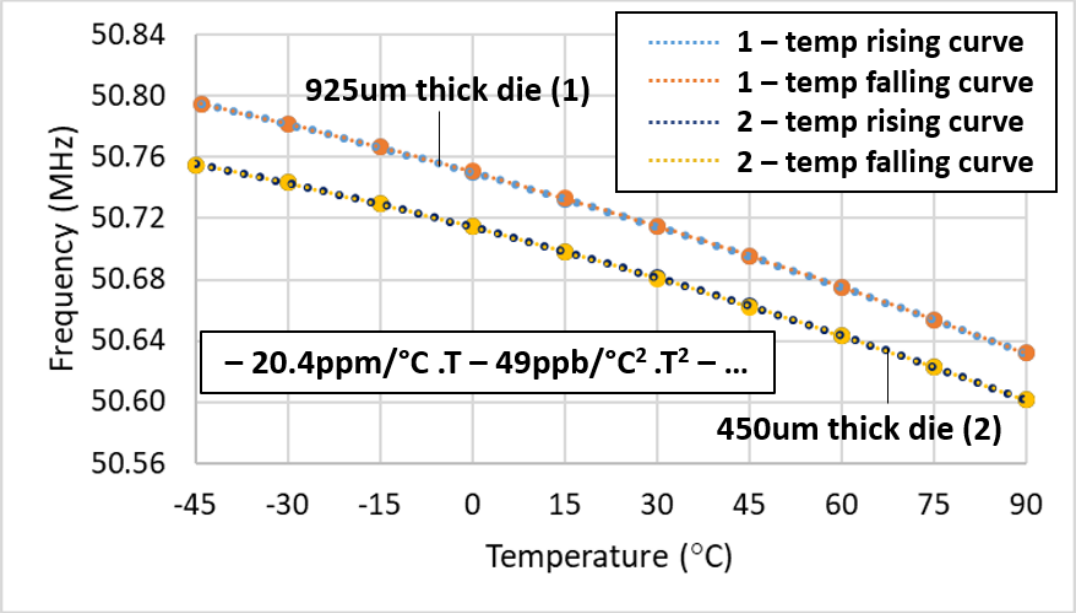

Figure 58 - Frequency-temperature cycling of both the encapsulated designs, showing negligible hysteresis of <500Hz between temperature rising and falling cycles with TCF1 and TCF2 of -20.4ppm/°C and -49ppb/°C^2 respectively.

Another WLP wafer was grinded down from the backside of the wafer from its original total thickness of 925µm to 450µm. Figure 57 shows the images of both the original and thinned DLR dies. The DLRs from the thinned wafer were measured and compared with the original device die. Temperature cycling experiments were carried out on both the 925µm and the 450µm dies across -45°C to 90°C. Results show that the thinning process did not cause any behavior drift in the resonator with both 925µm and the 450µm devices demonstrating consistence repeatable temperature behavior with negligible hysteresis <500Hz (10ppm) as shown in Figure 58. Both resonators show *Q*-factors of ~200k with less than 10% variations across the entire temperature range, which verifies the elimination of large TED with strong temperature dependency by conserving the property of undistorted Lamé mode. The thinning experiment verified the robustness of both the DLR design and the WLP process, showing promises for integration of thinned MEMS devices

on flexible substrate for advanced wearable applications. The wafer map of the frequencies, Q and insertion loss are shown in figure xx of the three wafers that were tested. Note that not all devices were tested on every wafer, some of the devices were not working, or lost in the dicing process.

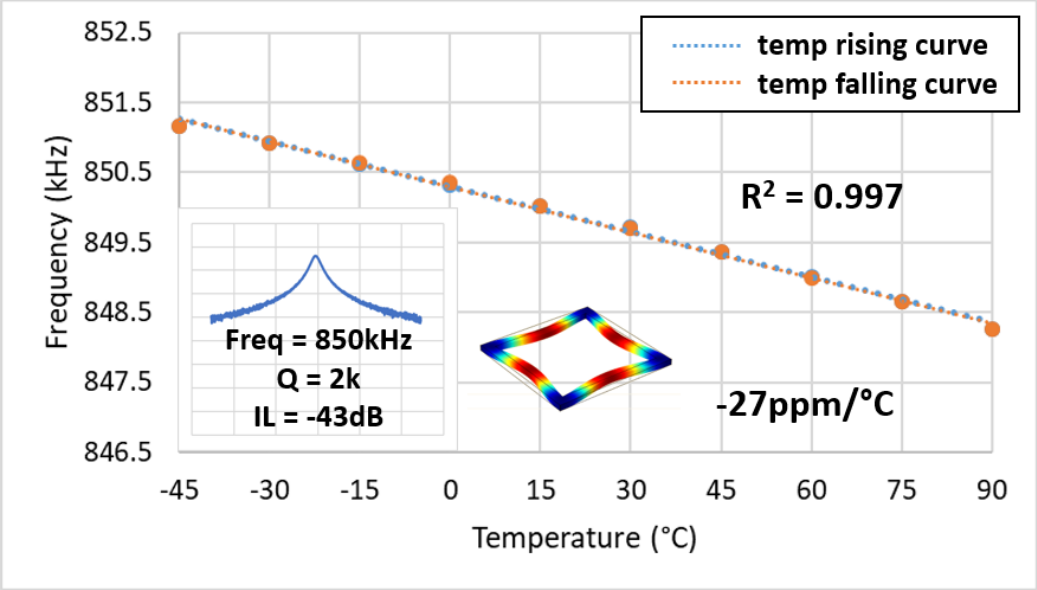

Figure 59 - Frequency characteristics of the lower frequency flexural mode at 850kHz showing linear TCF of -27ppm/°C, which may be used as a reference curve for temperature-stable OCXOs.

Another important feature for the DLR designs is the presence of a lower frequency flexural mode in the range of 100s of kHz to 10s of MHz, according to the length and width of their edge. The flexural modes usually have a linear negative temperature-frequency relationship and a TCF of about -27ppm/°C, as measured in the FDLR2 design, for which the flexural mode is at 850kHz with a *Q* of 2k, as shown in Figure 59. This allows us to make use of the linear TCF in the lower frequency mode as a frequency-output temperature sensor in temperature compensation of the higher frequency mode, for example in OCXOs which have been shown previously in literature [14], [82]. It is also observed that other

than the distributed Lame mode and the low frequency flexural mode, there are no other spurious modes for the frame configuration in the wide range frequency sweep between 600kHz to 60MHz, as shown in Figure 60, which ensures stable oscillator implementations. The temperature cycling results show that the DLRs may be used as reliable timing elements in high power circuits such as motherboards, where temperatures rise and fall frequently across a wide temperature range.

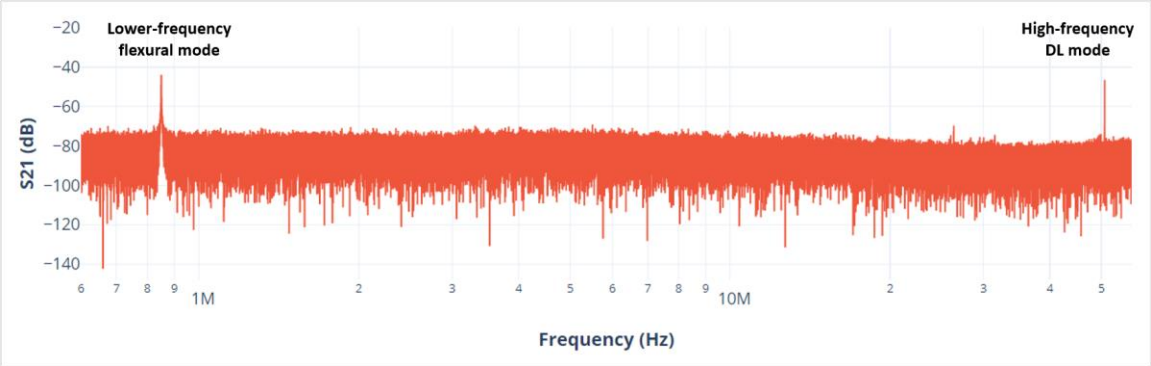

Figure 60 - Large frequency span from 600kHz to 60MHz, showing no spurious modes for the FDLR2 design.

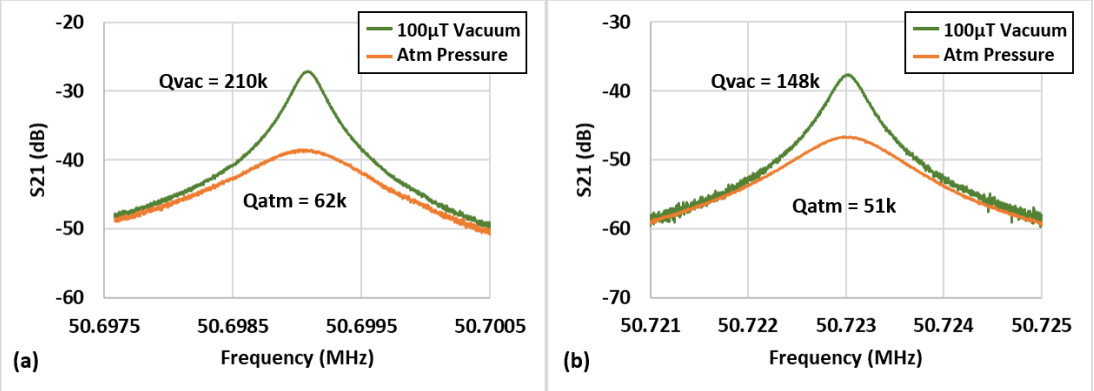

Figure 61 - Qs of (a) the frame and (b) beam DLRs of uncapped devices measured in vacuum and air, showing a slight degradation in air due to squeeze-film damping, but maintaining high Qs of 62k and 51k respectively, showing that these devices can also be operated at atmospheric pressure. The degradation of Q can be completely removed by designing these devices at a still higher frequency.

It is worth noting that owing to their high resonance frequencies, the DLRs do not require very low vacuum packaging below 1Torr, which would otherwise involve the use of getters and increase process complicity and cost. To verify this, uncapped frame and beam DLRs were tested in both a vacuum chamber with sub-mTorr pressure and in atmosphere. *Q*-factors of 148k and 210k were measured for the beam and frame DLRs, which matches the typical values seem on WLP dies with 1~10Torr pressure, indicating the air damping is not a limiting factor even in the WLP dies without getters. It was also seen that the corresponding *Q*-factors are 62k and 51k in atmosphere, for the uncapped frame and beam DLRs respectively. While squeeze film damping starts to contribute in atmosphere pressure, the *Q*-factors are still considered to be high enough for timing reference implementation, yielding low motional impedance of 7.8kΩ and 19kΩ for the frame and beam resonators respectively (Figure 61). Compared to conventional lower frequency resonators, which are sensitive to packaging pressure and may fail if the package vacuum is compromised [83], the high-frequency DLRs demonstrate much better robustness and reliability against extreme environment conditions.

4.3 Fabrication of Distributed Lame Mode Resonators

The DLR are fabricated on N-doped SOI wafers using the HARPSS process which enables sub-micron-gap capacitive transduction. 60μm (+/-1μm) and 40μm (+/-0.5μm) SOI were used to fabricate the beam DLR and frame DLR respectively. A frame DLR was also fabricated on a 45um (+/-2.5um) epitaxially-grown polysilicon substrate. It is important to note that the large thickness variation in the epi-poly substrate does not affect the frequency of the frame DLR owing to its robustness to thickness variation.

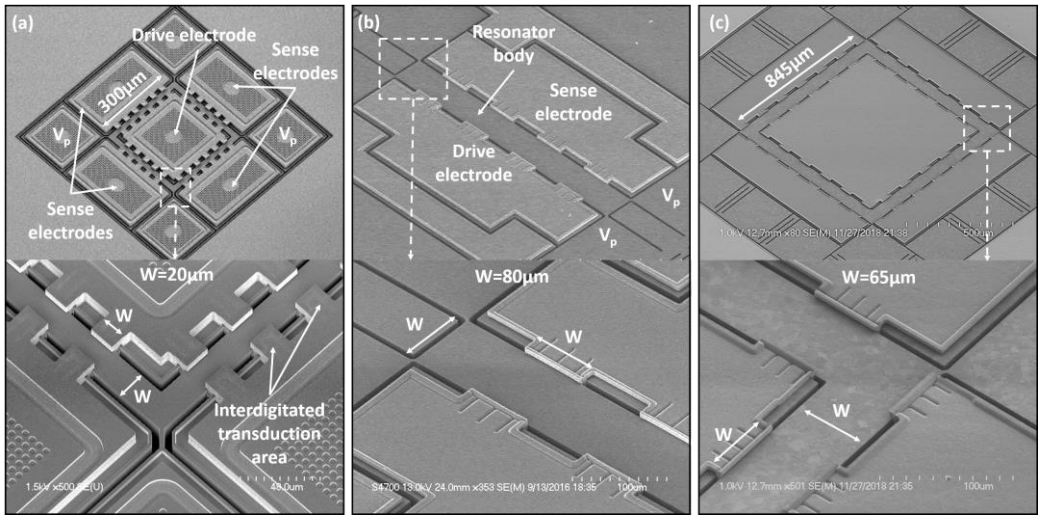

Figure 62 – SEM images of a silicon frame DLR (a), silicon beam DLR (b) and an epi-poly frame DLR (c) of various widths. Note that the unique discontinuous interdigitated electrode is required to actuate the distributed mode shapes, which is enabled by the HARPSS process for nano-gaps.

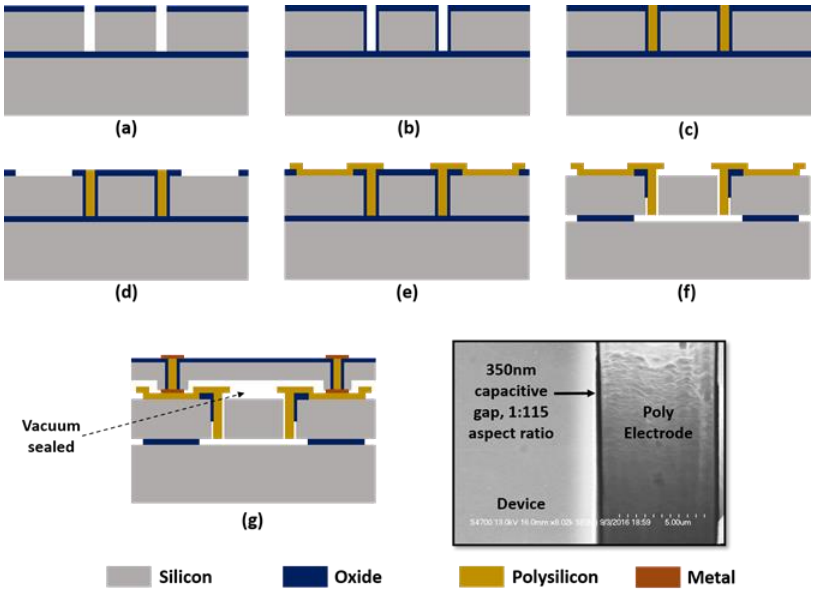

Figure 63 – HARPSS Process flow of DLR enabling nano-gaps of 350nm which result in an aspect ratio of 1:115 for the capacitive gaps, with a SEM image of the cross-section of the actual capacitive nano-gap within these devices.

Firstly, trenches are etched in the device layer of an SOI wafer by DRIE using an oxide mask Figure 63(a). An oxidation is done at 1100°C to form the nano-gaps on the sidewall

of the etched trenches (b). Next, in-situ doped LPCVD polysilicon is deposited at 588°C in the trenches by multiple depositions to mitigate the stress and then the polysilicon is etched back to the surface from the top and bottom of the wafer (c). The top oxide is then patterned to open out the electrodes where there needs to be a contact to the silicon device layer (d). LPCVD polysilicon is then deposited again using the same conditions as step (b), to form the connections with the silicon and the vertically deposited polysilicon in the trenches (e). Next, the polysilicon is etched from the trenches other than the electrode regions and finally the device is released in 49% HF (f). Note that for the epi-polysilicon substrate, the same process is followed, albeit at a reduced temperature to minimize the stress in the released devices [84].

4.3.1 High Aspect Ratio Vertical Poly Etching

While the process needed to fabricate the DLRs is quite straightforward, one of the key aspects involved is the etching of the unwanted poly from the trenches where HARPSS electrodes are not present. During the poly filling steps, every single trench on the entire wafer would be filled, however we only want polysilicon to be present in the regions where the capacitive gaps are required. Hence, we need to etch away the poly from the other regions, which is most of the trench regions on the wafer.

This step is quite difficult, considering the residue formation of polysilicon and excessive teflon during the etching process. However, this is especially challenging while fabricating DLRs, since we have a digitated electrode, where the area between the digits is very small. This means that in order to effectively etch that area, we need to characterize a recipe that can etch a higher aspect ratio of polysilicon as compared to the rest of the

trenches. This region is especially small for example for a 167MHz resonator, it would be required that the etch would be barely 20um in length and 40um in depth. While this kind of etching is relatively easy to do in SCS, etching a trench filled with polysilicon becomes extremely challenging. Hence, some parameters of the initial vertical poly recipe need to be modified to account for this high aspect ratio. Furthermore, the rest of the wafer still holds wider regions for poly etching, so the same recipe must also be suitable for those trenches. A third point to be noted, is that some regions consist of polysilicon overhangs, where there are regions where only 4-5um of poly thickness is supposed to be etched. However, these regions are subject to the entire process which is used to etch the 40um deep vertical poly as well. This results in under-cutting of those overhangs and it must be done carefully so that the undercut is not large. These points are explained clearly in Figure 64. Similar to the earlier vertical poly etching step, STS HRM is used for this recipe as well. The only change in the two recipes is the time ramping, which in this case must not be large for the etch cycle. A large etch cycle time would result in heavy undercuts for both the poly overhangs and also the adjacent electrode walls. However, this results in more poly residues in terms of striations and thus the recipe has to be followed in multiple steps and changed accordingly after every etch. The recipe is given in Table 14.

Table 14: Vertical poly etching recipe in STS HRM for DLRs

Parameter	**Value**	
	Etch	Passivation
Cycle time (s)	4 to 6.5	2
Throttle mode, position (%)	Manual, 83	Manual, 83
Gases (sccm)		

C_4F_8	0	200
SF_6	200	0
O_2	20	0
13.56MHz Coil power (W)	2000	1200
LF Platen power (W)	80	0
Platen power ramp (W/min)	0	0

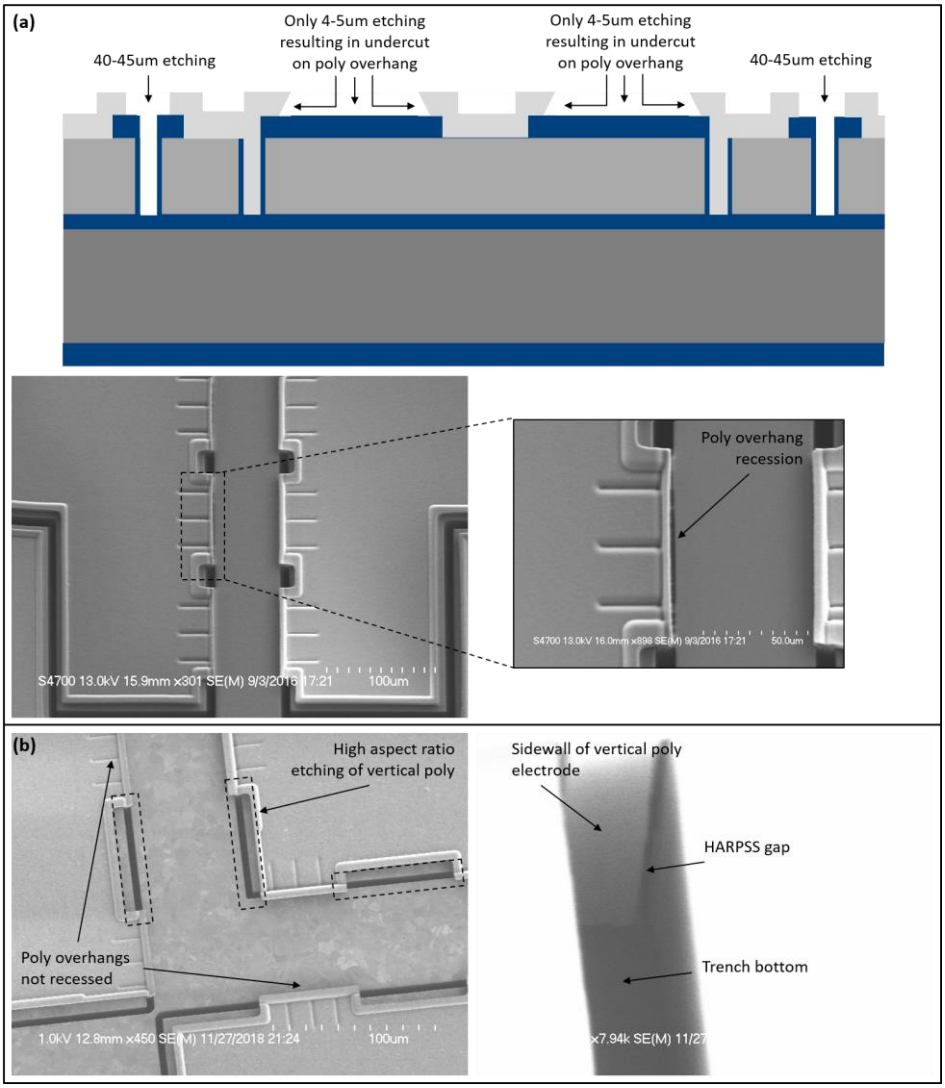

Figure 64 – Pictorial representation and SEM images of different poly regions being etched at the same time (a) which causes the poly overhangs to be undercut because of over etching; SEM images of the poly overhang not recessed and high aspect ratio vertical poly regions in the DLR due to its design which don't usually exist in other devices (b).

CHAPTER 5. PIEZO-CAPACITIVE BAW ACCELEROMETER USING A GAP-CHANGING MOVING ELECTRODE

Capacitive IMUs and accelerometers have played an influential role in navigation and high-performance motion sensing since the advent of the inertial MEMS industry due to their small size, low power, and large electromechanical sensitivity [85], [86]. However, in order to have a large sensitivity, most commercial accelerometers have a relatively low resonant frequency [87]. Hence, accelerometers operating at small levels of g have a large device stiffness which makes them low bandwidth due to their static nature [88], [89]. There have also been attempts at improving the capacitive sensitivity by using hinged shaped electrodes [90]. Therefore, it becomes imperative to design an accelerometer that is stiff, as well as capable of sensing small accelerations. To overcome the low sensitivity of the stiff proof mass at small accelerations, we use the concept of a gap changing moving electrode, which reduces the gap size, thereby increasing the capacitive sensitivity. There has been prior work on resonant accelerometers, with resonant frequencies being in the order of hundreds of kHz, showing large sensitivity [91], [92] and high *Q*-factors [93], however these have considerably small dynamic ranges. Extending the dynamic range is important so that the same device can be used for high-g (military) as well as low-g applications (seismic detection). In our work, a high-frequency accelerometer is fabricated using the piezo-HARPSS process, which relies on the electrostatic frequency tuning of a piezoelectrically-actuated silicon BAW resonator with high stiffness, high resonant frequency, and high *Q*-factor. We can then improve the dynamic range using a moving electrode, which allows a gap-changing mechanism.

While capacitive transduction used in the conventional HARPSS process is effectively used for devices requiring large quality factors, there may be certain applications where other parameters such as low insertion loss, larger displacements, robustness and lower feedthrough also are of primary importance. Hence, piezoelectric transduction may be required to achieve them at the cost of *Q*. A BAW resonant accelerometer is one such device, where compared to conventional mechanical-stiffness-based resonant accelerometers, this technique presents better linearity, high frequency of operation and better performance scalability. However, for output frequency sensing, we require a robust, low noise mechanism which eliminates acceleration induced vibrations in the oscillator loop. Hence, we use piezoelectric transduction for the sensing (frequency tuning), which decouples itself from the actuation of the device. Further, it enables low phase noise oscillators due to efficiency of the piezoelectric transducers (lower motional resistance) compared to capacitive transducers. Hence, to realize the combined piezo-capacitive actuation technology, a reduced-temperature variation of the HARPSS process must be used. Owing to the stable nature of piezoelectric transduction to get *Q*s of up to 10k, when combined with capacitive nano-gaps, one can fabricate devices such as a BAW accelerometer.

5.1 BAW Accelerometer Design

The BAW accelerometer consists of a suspended electromechanical system that resonates in a BAW mode, flexural tethers anchoring the BAW resonator, and a tuning airgap electrode placed close to the bulk resonator forming a small capacitive tuning gap (Figure 65). The resonator is actuated to oscillate in a high-frequency BAW mode, the frequency of which will be used as acceleration indicator. Stiff tethers rigidly suspend the

resonator at the nodes of the BAW mode. Linear accelerations will cause a small translational displacement of the resonator, resulting in a gap-size change between the resonator and the tuning electrode, as a result, the resonant frequency of the BAW mode will change due to the change in electrical spring softening effect. To decouple actuation and sensing (nano-gap tuning) mechanism and to improve sensor stability, we incorporate thin film piezoelectric transduction for the actuation and readout of the BAW accelerometer. The salient features of the design are explained below:

5.1.1 High Stiffness BAW Structure

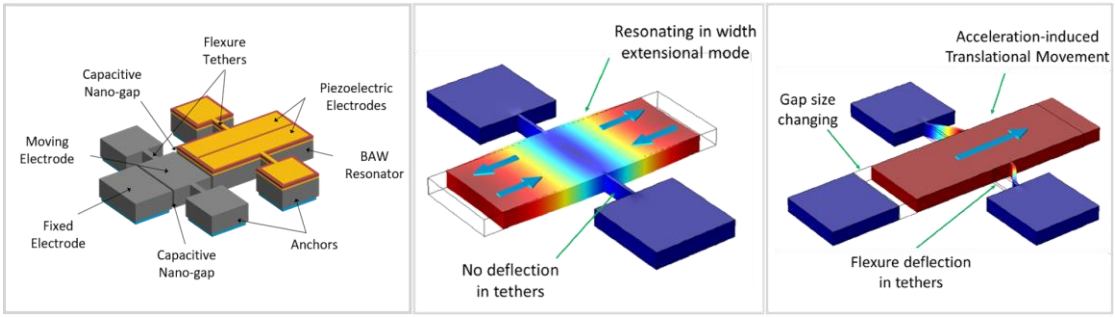

Figure 65 – (Left) Typical structure of a BAW accelerometer; (middle) deformation of the bulk acoustic wave resonant mode; (right) acceleration-induced deflection of the proof mass.

To use the BAW accelerometer as a high frequency device operating at large accelerations, it is imperative that the device should have a large stiffness to be insensitive to stray vibrations. Hence, the proposed BAW structure is designed to operate in a 2nd order length extensional (LE) mode. A higher order BAW mode enables proper anchoring of the bulk structure at multiple nodal points, mitigating cross-axis sensitivity and improving rotation rejection of the device. The entire sensor will have stiff tethers and high

resonance frequency, ensuring very small displacements even at large accelerations, large bandwidth, and high robustness.

The bulk acoustic wave mode is essentially independent of the anchoring tethers and can have high *Q*-factors exceeding 50,000 without needing high vacuum [67]. The combination of high resonance frequency and high *Q*-factor provides very low phase noise, which enables superior frequency resolutions. The BAW resonator also serves as a proof mass and forms another electromechanical system together with its anchoring tethers. It experiences a uniform deflection when an acceleration is applied. The magnitude of the deflection is determined by the total mass of the BAW resonator and the spring constant of the tethers and is independent of the BAW resonant mode. The acceleration-induced deflection causes a change in the capacitive gap between the movable BAW resonator and the tuning electrode, altering the electrostatic spring constant K_E. The mechanical spring constant of the BAW resonator K_{BAW} remains constant during acceleration-induced motions, so that the overall stiffness change is caused by changes in K_E. The electrostatic spring constant is given by:

$$K_E = \frac{-\varepsilon A V_t^2}{d^3} \tag{13}$$

Here V_t, A, and d, are the tuning voltage, area of the tuning capacitor and capacitive gap-size respectively. The corresponding resonance frequency of the BAW resonator is:

$$f_{electromech} = \frac{1}{2\pi}\sqrt{\frac{K_{BAW} - K_E}{M_{effective}}} = f_{BAW}\sqrt{1 - \frac{\varepsilon A V_t^2}{K_{BAW} d^3}} \tag{14}$$

where f_{BAW} is the un-tuned resonance frequency of the BAW mode. The acceleration-induced deflection of the bulk structure (figure 38, right) is given by:

$$\frac{\partial d}{\partial a} = \frac{M_{proofmass}}{K_{flex}} = \frac{1}{\omega_{flex}^2} \tag{15}$$

where $M_{proofmass}$, K_{flex}, and ω_{flex} are the total mass of the BAW resonator, spring constant of the tethers and angular frequency corresponding to the translational mode of the bulk structure respectively. For a small change of ∂d in gap size due to external acceleration, the scale factor of the BAW accelerometer can be derived as:

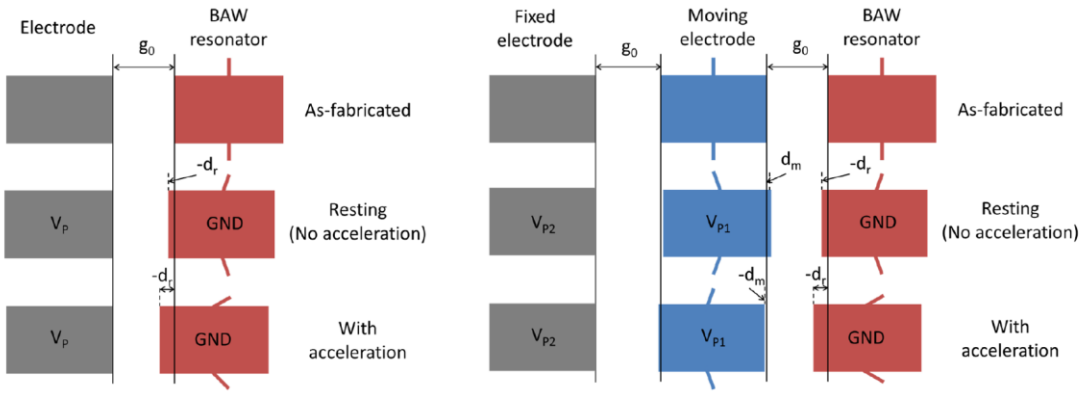

Figure 66 – Pictorial representation of the motion of the accelerometer during acceleration in the case of only a fixed electrode (left), and by addition of a moving electrode between the fixed electrode and the accelerometer (right).

$$SF = \frac{\partial f_{electromech}}{\partial a} = \frac{1}{\omega_{flex}^2} f_{BAW} \frac{1}{2}\left(1 + \frac{\varepsilon A V_t^2}{2K_{BAW} d^3}\right)\frac{3\varepsilon A V_t^2}{K_{BAW} d^4} \tag{16}$$

Since the accelerometer scale factor (SF) is approximately proportional to $1/d^4$, it increases significantly with smaller gap sizes. In order to achieve a very small gap size, HARPSS process can be used in fabrication, which enables high aspect ratio nanoscale capacitive

gaps. Also, because the sensitivity is inversely proportional only to the first order of K_{flex}, the same sensitivity can be achieved with 16 times stiffer tethers if the gap size is reduced by a factor of two. Consequently, the acceleration-induced deflection can be significantly reduced without degrading the sensor resolution using small initial gap size, leading to large full-scale range and extremely high shock and vibration resistance.

5.1.2 Moving Electrode Design

The novel moving electrode concept will be used to expand the linear dynamic range of the device. The tuning electrode undergoes a nonlinear displacement under the action of acceleration and electrostatic force, which automatically counteracts the frequency-tuning induced nonlinearity, resulting in a more linear scale factor. The moving electrode is self-acting and requires no active control electronics or close-loop operation. This will enable significantly larger dynamic range (up to 10^9) and ultra-high shock resistance, providing coverage of a large range by using a single device.

For a simple resonant accelerometer with fixed tuning electrode, a trade-off between the resolution and scale factor linearity always exists because of the nonlinear nature of electrostatic tuning, limiting its linear dynamic range. As seen in (14), the tuning frequency is a non-linear function of displacement. As the capacitive gap reduces, the frequency drops faster for the same acceleration increment, causing large scale factor nonlinearity at high acceleration input. If we also consider the electrostatic force, it is given by:

$$F_E = \frac{\varepsilon A V_P^2}{2} \frac{1}{(g_0 + d_r)^2} \tag{17}$$

Thus, the electrostatic force increases when the gap size decreases, causing the displacement to increase nonlinearly with acceleration. It adds to the nonlinear frequency tuning and leads to even larger scale factor nonlinearity.

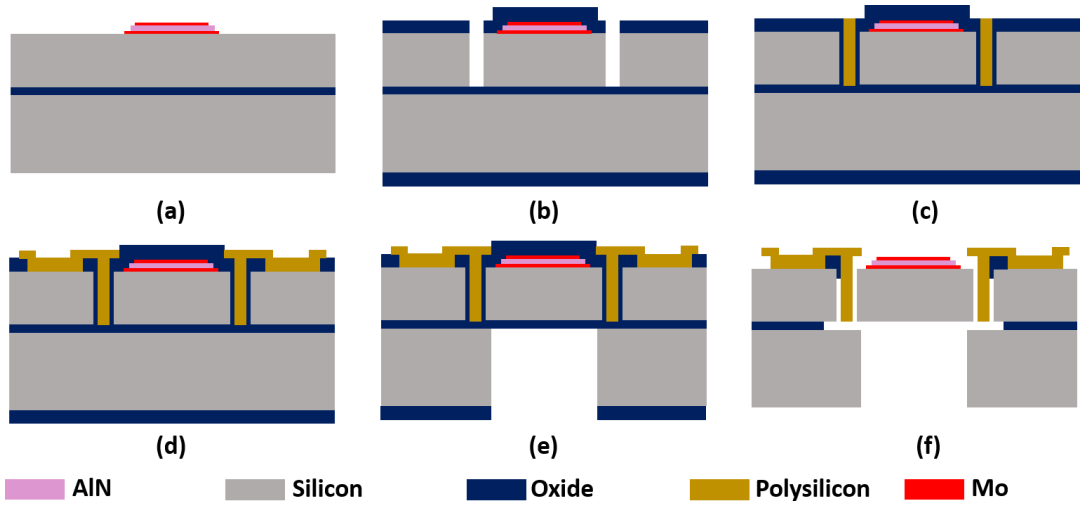

Figure 67 – Process flow for piezo-HARPSS BAW accelerometer.

However, by introducing a moving tuning electrode, the electrostatic force nonlinearity can become favorable and improve the overall linearity of the scale factor. The electrostatic forces F_{fm} and F_{mr} are thus given by:

$$F_{fm} = \frac{\varepsilon A (V_{P1} - V_{P2})^2}{2} \frac{1}{(g_{fm})^2} = \frac{\varepsilon A (V_{P1} - V_{P2})^2}{2} \frac{1}{(g_0 + d_m)^2} \tag{18}$$

$$F_{fm} = \frac{\varepsilon A (V_{P1})^2}{2} \frac{1}{(g_{mr})^2} = \frac{\varepsilon A (V_{P1})^2}{2} \frac{1}{(g_0 + d_r - d_m)^2} \tag{19}$$

where d_r and d_m are the displacements of the resonator and the moving electrode, g_{fm} and g_{mr} are the effective gaps between the fixed and moving electrode and the moving electrode with the resonator respectively. V_{P1} and V_{P2} being the DC voltage applied to the moving

and fixed electrodes. Both electrostatic forces have nonlinear dependency on the acceleration-induced displacements and increase with larger acceleration input. Similar to the simple fixed electrode case, the increasing F_{mr} causes the tuning gap g_{mr} to close faster at higher acceleration, which will add to the frequency tuning nonlinearity. However, the increase of F_{fm} with larger acceleration will cause the tuning gap g_{mr} to close slower, which counteracts the frequency tuning nonlinearity. With proper design, the change of F_{fm} may dominate the electrostatic force nonlinearity, therefore enabling a self-acting nonlinearity cancellation (Figure 66).

5.1.3 Combined Capacitive and Piezoelectric Transduction

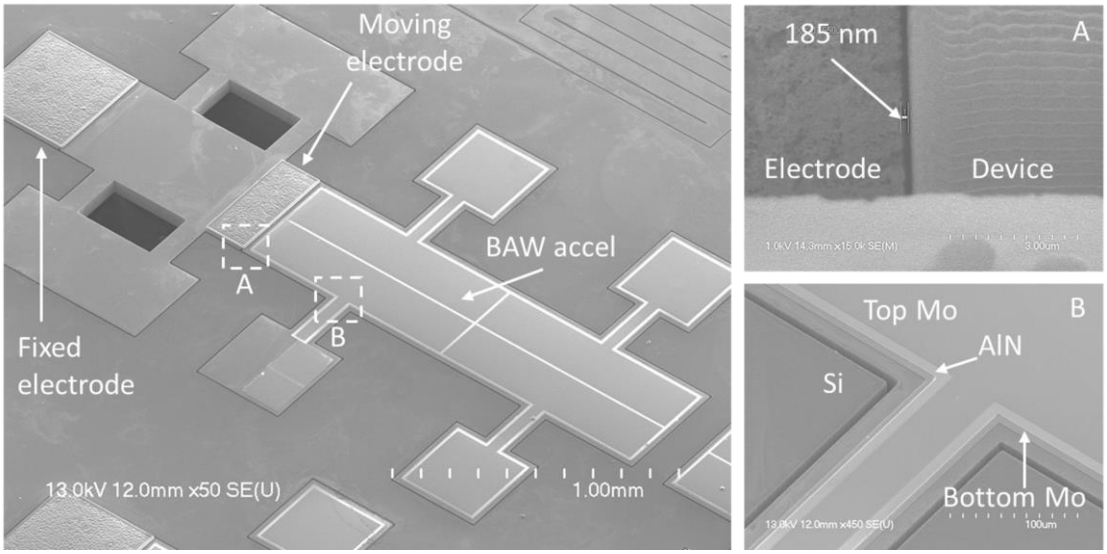

Figure 68 – SEM images of the fabricated 2nd order LE BAW accelerometer; (A) close up of the 185nm HARPSS gap and (B) the Mo-AlN-Mo piezo stack.

After the resonating structure is designed, it is important to realize the transduction mechanism to be used for the device. Capacitive transduction enables the electrostatic spring-softening-based sensing mechanism. Compared to conventional mechanical-

stiffness-based resonant accelerometers, this technique presents better linearity, high frequency of operation and better performance scalability. However, for output frequency sensing, we require a robust, low noise mechanism which eliminates acceleration induced vibrations in the oscillator loop. Hence, we use piezoelectric transduction for the sensing (frequency tuning), which decouples itself from the actuation of the device. Further, it enables low phase noise oscillators due to efficiency of the piezoelectric transducers (lower motional resistance) compared to capacitive transducers. The fabrication process is explained in the next section.

5.2 Reduced-temperature Process for Piezo-HARPSS Devices

The process flow is shown in Figure 67. The Mo-AlN-Mo piezo stack was first etched using 3 masks for each layer (Figure 67a). The Mo is patterned and etched in a recipe containing SF_6 and O_2. The AlN is then wet-etched using MF-319 developer at 40°C. The bottom Mo is then etched in the same way as the top Mo, using resist mask. Then, a 3um layer of PECVD oxide is deposited on the surface of the wafer, and trenches are etched into the 60um device layer (b). Care must be taken that the footing in this step is as less as possible and this is done by checking under IR microscope from the back side of the wafer. Next, a thin sacrificial oxide for the nano-gap is deposited using TEOS at 725°C. In-situ doped LPCVD polysilicon is then filled into the trenches at 588°C and etched back after every deposition of 1.4um. The polysilicon is to be etched back after every deposition (c). The next step is to then etch away the oxide from the surface to open up the silicon surface for top poly contact. Top poly is then deposited once, similar to the trench filling step (d). Then, the poly is etched away from the trenches defining the device, only to leave the poly in places where we have electrodes. Then, backside holes are etched from the handle layer

of the wafer, which must be larger than the device, to reduce the release time (e). Finally, the devices are released in BOE, to prevent the peeling of the piezo-stack from HF release (f).

5.2.1 Delamination of Mo Electrodes

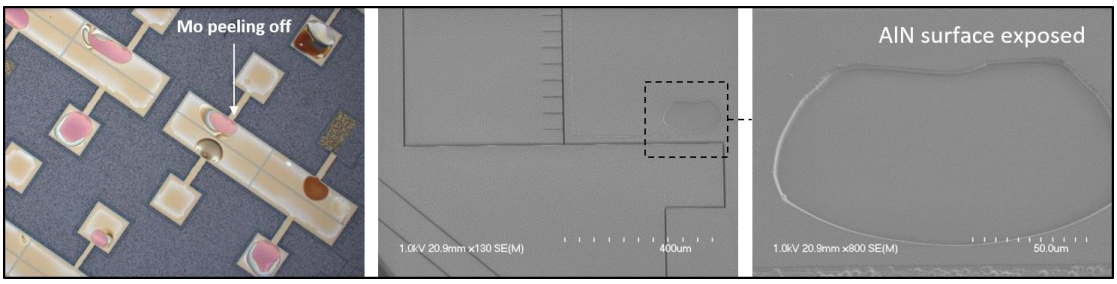

Figure 69 – Optical (left) and SEM (center, right) images of Mo electrodes peeling off due to pin-holes in the PECVD film, or incompatibility with deposited oxide or LPCVD polysilicon.

While the earlier process flow was successfully used to fabricate a compatible piezo-capacitive process, there were many issues that brought about a reduction in yield. One of the major drawbacks is the use of Mo electrodes for the piezoelectric AlN film. Even though the temperature of the process had to be reduced to accommodate the metal electrodes, they were incompatible with the deposition of PECVD oxide and then LPCVD polysilicon on them. Another issue with the use of metal, is the inability to use cleaning acidic agents such as piranha, EKC, etc., which degraded the fabrication cleanliness, further affecting yield. By the end of the process, several of the Mo electrodes were delaminated or peeling, and almost all the electrodes had portions of Mo broken. This is shown in Figure 69, where one can clearly see the delamination, exposing the AlN below.

5.3 Metal-less Piezo-capacitive Process for Piezo-HARPSS Devices

In order to overcome these issues, a different process had to be designed. For this purpose, it was imperative that there needed to be a substitute for the metal in the process, so as to allow higher temperatures to be compatible and also to use cleaning agents in order to improve the yield of the process. Hence, the metal electrodes were substituted by LPCVD polysilicon itself, the same film that was used to create the capacitive nano-gaps in the HARPSS process. This allowed the same number of masks to be used but eliminated the issues that were caused during processing by the presence of metal, viz, Mo electrodes.

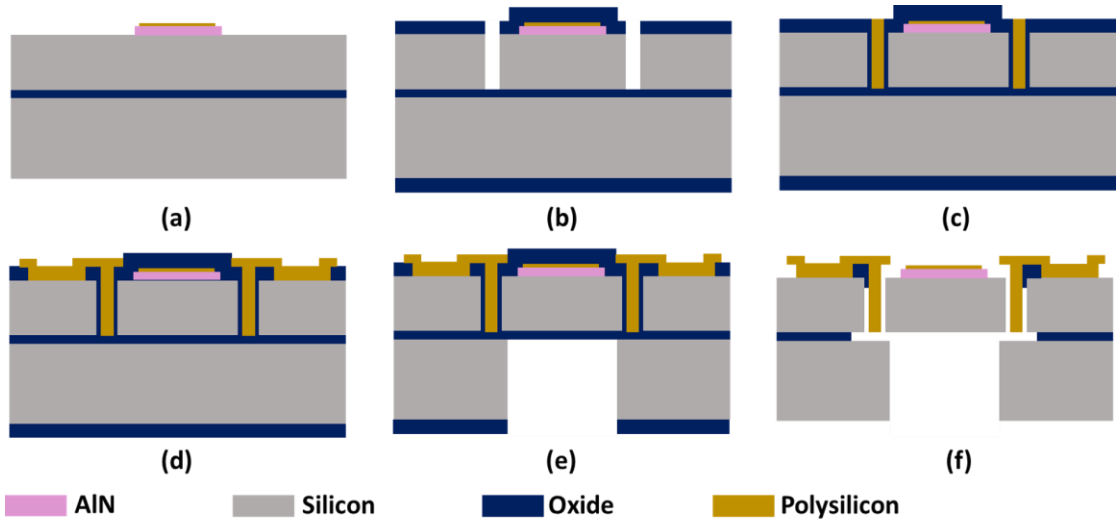

Figure 70 – Metal-less piezo-capacitive HARPSS process flow.

The process flow is shown in Figure 70. The wafers were sent to an external source to deposit AlN films. While in the earlier process the external foundry deposited the entire piezo stack containing Mo-AlN-Mo, in this case we didn't need the Mo electrodes. By depositing the AlN directly on Si, it was required that the Si device layer had to be highly doped, in order for the substrate itself to work as the bottom electrode. The silicon device layer was <0.005 ohm-cm N/As doped. Firstly, 1um of PECVD oxide was deposited at the back of the wafer. A thin layer of 300nm of LPCVD polysilicon was deposited on the AlN

film which would serve as the top layer. Then, this layer and the AlN layer below were patterned as shown in (a). After that, the top of the wafer was covered with 2-3um of PECVD oxide to form the main mask for the corresponding HARPSS process to follow. Trenches were etched into the device layer (b) and a 90nm of sacrificial oxide was grown at a lower temperature of 900°C. Then, similar to the conventional HARPSS process, LPCVD in-situ doped polysilicon was deposited into the trenches at 588°C and etched back to the surface (c). Next, the top oxide was etched to form the electrode connections and top poly was deposited using the same conditions as earlier (d). The unwanted polysilicon was then etched from the trenches and the surface, forming the HARPSS electrodes. It must be noted that this whole procedure did not cause the AlN and the thin poly used as electrodes to delaminate or peel off. Then, PECVD oxide of upto 4-5um was deposited on the backside of the wafer and the backside holes were etched for release (e). Finally, the devices were released in 49% Hf (f).

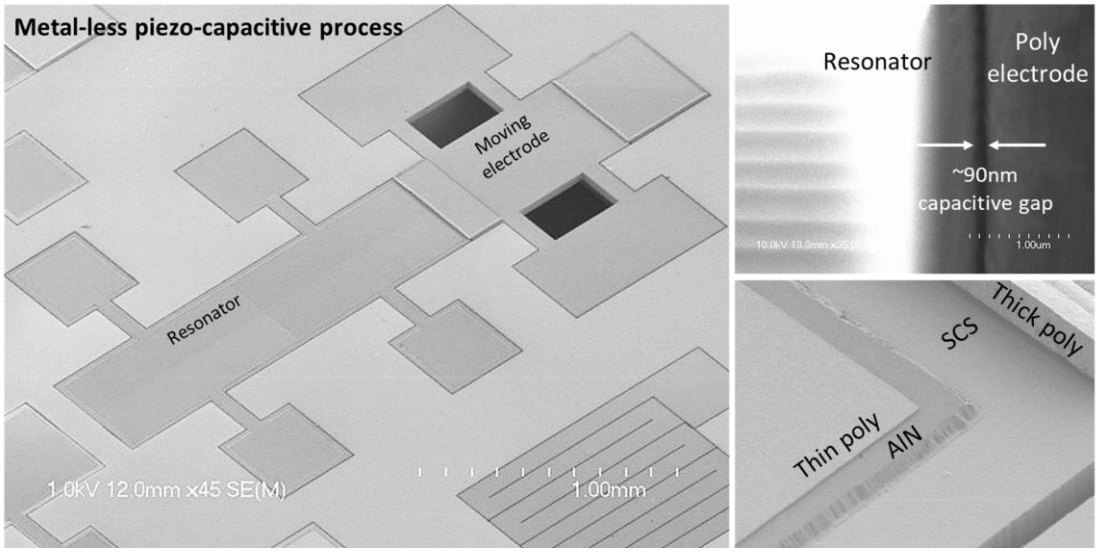

Figure 71 – SEM images of the fabricated 2nd order LE BAW accelerometer using the metal-less process. Insets also show the 90nm HARPSS gap and the piezo stack comprising of the top polysilicon electrode and AlN layer.

5.3.1 Dry Etching of AlN

One of the important issues that were improved drastically during this process is the etching of the AlN. In order to fabricate nano-gaps in the order of sub 100nm, it is essential to have fairly smooth sidewalls while etching the trenches itself. Generally, AlN is wet-etched using a solvent containing TMAH such as MF319 developer or can be etched by KOH and IPA. While this works well for thin AlN films and smaller areas, it was seen that using this recipe for larger areas and thick films, resulted in a lot of residue on the wafer. This residue was detrimental to the steps ahead, because it micro-masked the trenches that were etched in the later steps. This micro-masking created major non-uniformity in the etching of the sidewalls. The Figure 72 shows the effect of this.

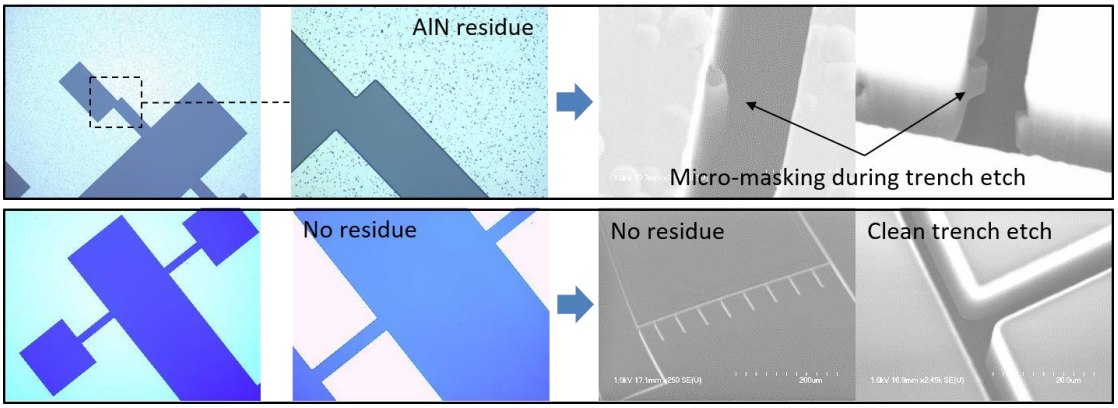

Figure 72 – AlN residue generated due to wet-etching which results in non-uniformities in the trenches due to micromasking (top); residual issues solved by using dry etching for AlN, resulting in smooth sidewalls and cleanly etched trenches (bottom).

To overcome this issue, the AlN film was dry etched. While dry etching also creates some roughness on the silicon substrate, its effect is not detrimental to the etching of the trenches. The Plasma-Therm ICP was used for this process, the recipe is shown in Table 15. There was a significant improvement in the etching quality, as can be seen in the bottom

images of the Figure 72. This allows the trenches to be etched cleanly in the following steps and helps us enable sub 100nm nano-gaps for the completed devices.

Table 15: AlN dry etching recipe in PT ICP

Parameter	Value
Turbo Pressure (mT)	5
Cl_2 (sccm)	40
BCl_3 (sccm)	10
Ar (sccm)	10
RF1 (W)	100
RF2 (W)	250
Helium Cooling	ON

5.3.2 Sac-ox Protection on Trench Sidewall

Another interesting feature that was noticed during this particular process was the etching of the oxide on the sidewall of the trenches during polysilicon etch-back. This is not an issue in conventional HARPSS processes, considering much larger gap sizes in the order of 250-300nm, however, in this current process, the gap size is 90nm, which causes difficulty in poly etch-back. The issue can be explained in detail as in the Figure 73. When LPCVD polysilicon is deposited for trench filling, generally it is better to etch-back this polysilicon to the surface between every deposition. The advantage of doing this is that it opens out the pinching-off at the top of the trench caused by the nature of LPCVD deposition and also creates a positive taper in the trench which prevents voids being formed in the trench refill. However, for smaller sub-100nm gaps, the sacrificial oxide on the

sidewall is extremely thin. Hence during etch-back steps, there is a chance that this oxide might get etched and the poly which is refilled will get shorted to the adjacent silicon, which will be detrimental to the process.

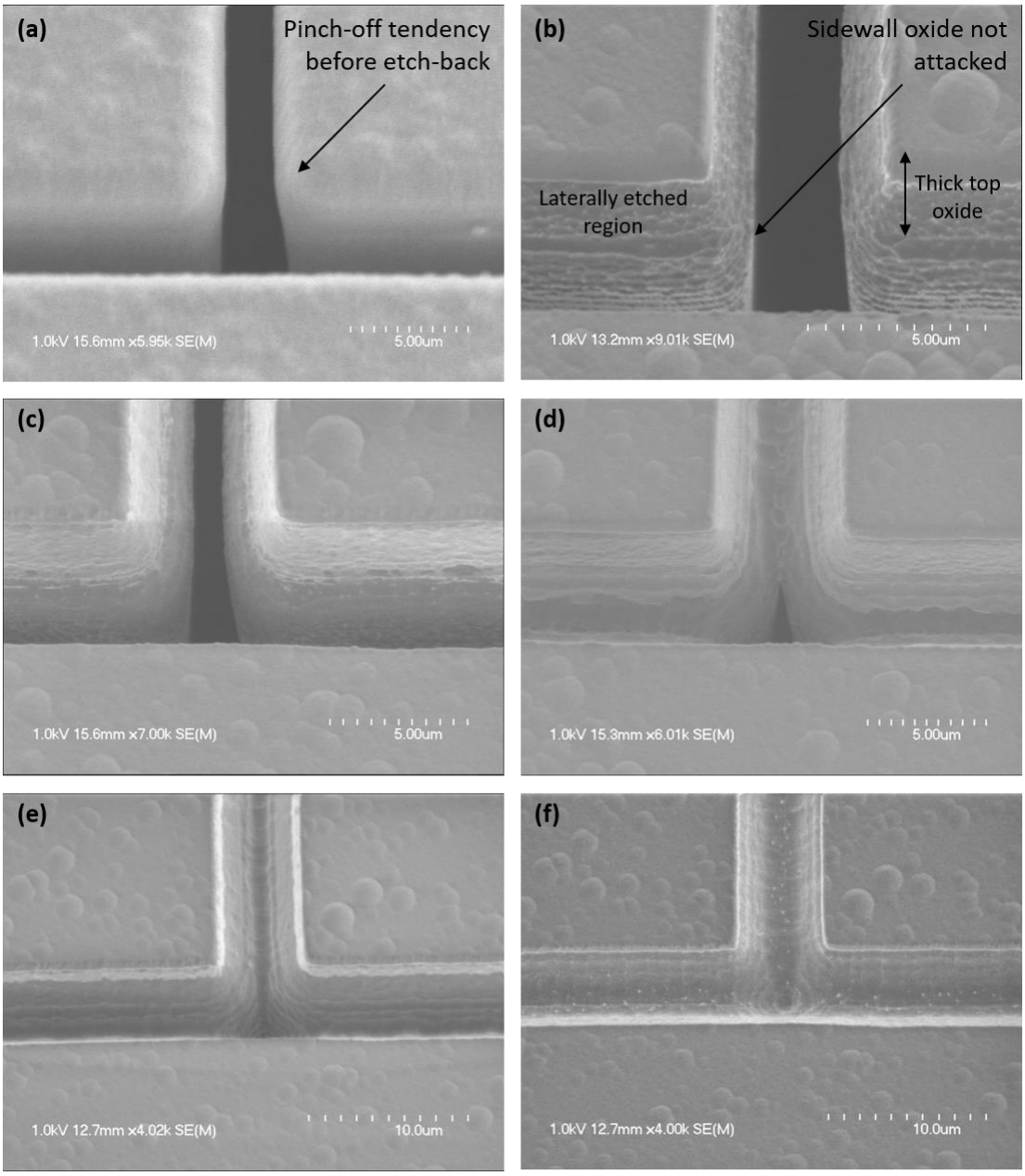

Figure 73 – A pinch-off tendency for the poly while filling trenches (a), after the first etch-back but using a large oxide top mask so that the poly isn't etched fully near the

oxide sidewall (b), corresponding trench fill steps after 5 depositions and etch-backs with the oxide on the sidewall fully protected in this step (c-f).

In order to avoid this, care must be taken during the etch-back steps so as to not over-etch the polysilicon. One way of doing this is to use a much thicker PECVD oxide mask, to give more margin for error during etch-back steps. For example, a 3um oxide on the top would give a larger margin for lag in the poly etch-back as compared to a 2um oxide, which might otherwise be considered thick enough to complete the HARPSS process. Another way of mitigating this effect is to etch-back every two poly depositions as compared to every deposition. While this increases the chances of voids inside the trench, it will not allow the oxide at the sidewall get exposed during the etch-back step. A combination of the thicker oxide mask and etch-back every second deposition can help eliminate this issue. Figure 73 shows a step-by-step demonstration of how we can protect the oxide sidewall from being attacked during the poly etch-back steps.

5.4 Characterization and Testing of BAW Accelerometer Devices

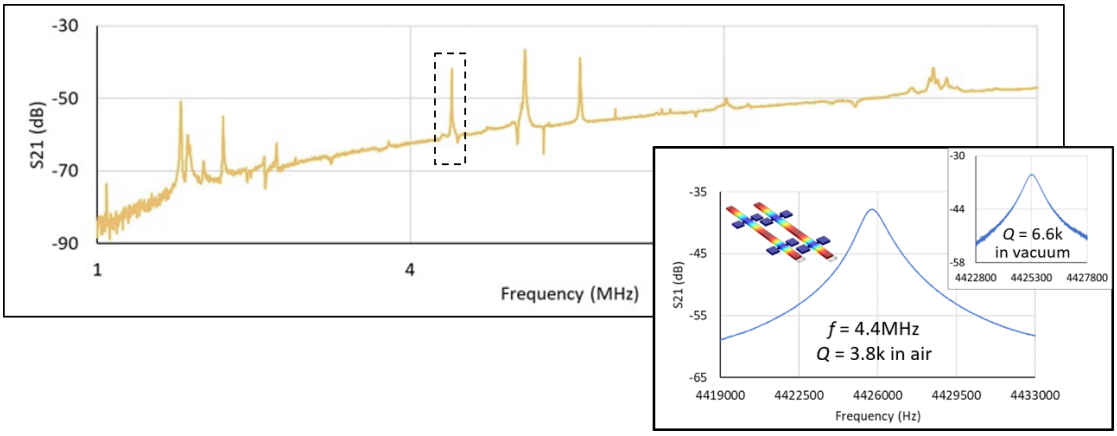

Figure 74 – Measured large-span frequency range and close up of the resonance peak of the fabricated BAW accel at 4.4MHz with a Q of 3800.

A batch of the prototype accelerometers were fabricated on the AlN-HARPSS platform with intended dynamic range of 50ug to 50g. *Q* as high as 6k is measured in vacuum on fabricated devices. Despite the 90 nm gap, the squeeze film damping was relatively low due to high frequency of operation at 4.4MHz, measuring a *Q* of 3800 in air, also verifying the advantage of using piezoelectric transduction to reduce necessary capacitive transduction areas (Figure 74). The operation in air is an important feature of this device, since it makes the setup and testing much easier by avoiding heavy vacuum tools. This is also another advantage of using piezoelectric transduction for the frequency measurement, since if the readout mechanism was capacitive, we would certainly need a vacuum environment to test this device.

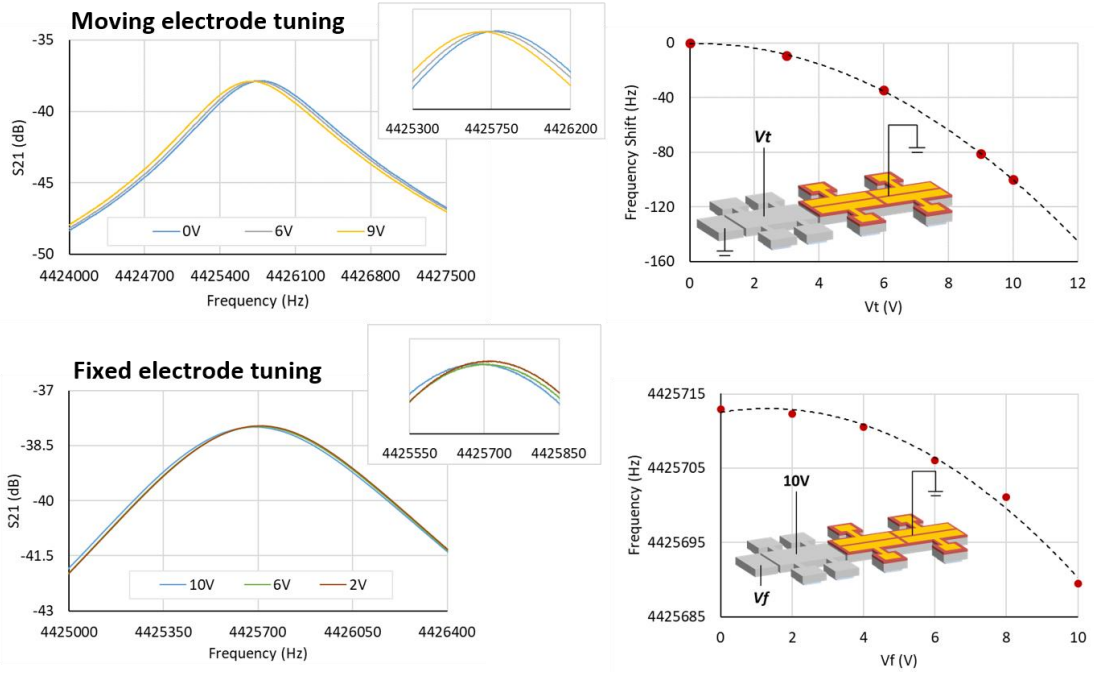

Figure 75 – Moving electrode functionality showing tuning of resonance frequency by moving electrode alone (top), a combination of moving and fixed electrode (bottom).

The moving electrode functionality was verified by a frequency tuning by applying voltages to mimic the force due to acceleration during actual testing. A tuning of about 4ppm/V of the BAW mode is observed when the resonator and the fixed electrode are kept at 0V, while applying a voltage V_t to the moving electrode. Then, a second dc voltage V_f is applied to the fixed electrode, while keeping the voltage at the moving electrode to be constant at 10V. Increasing V_f reduces the electrostatic force between fixed and moving electrodes. This causes the moving electrode to be drawn closer to the resonator, thereby reducing its frequency (Figure 75). A correct trend in frequency tuning shows that the moving electrode is working and can be an effective way to improve the dynamic range of the device. It should be noted that the frequency shift is extremely small and comparable to temperature drifts in the atmosphere, and hence there may be some errors in the measurement of the actual frequency tuning values.

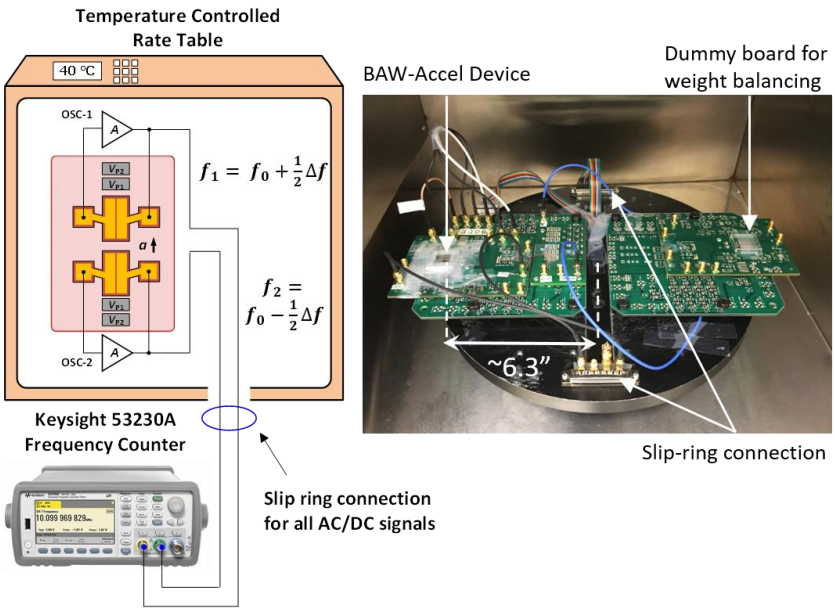

Figure 76 – (left) schematic diagram of testing setup for a differential pair of BAW accelerometers; (right) picture of testing setup with slip rings. A rate table was operated at a centrifugal acceleration of 10g.

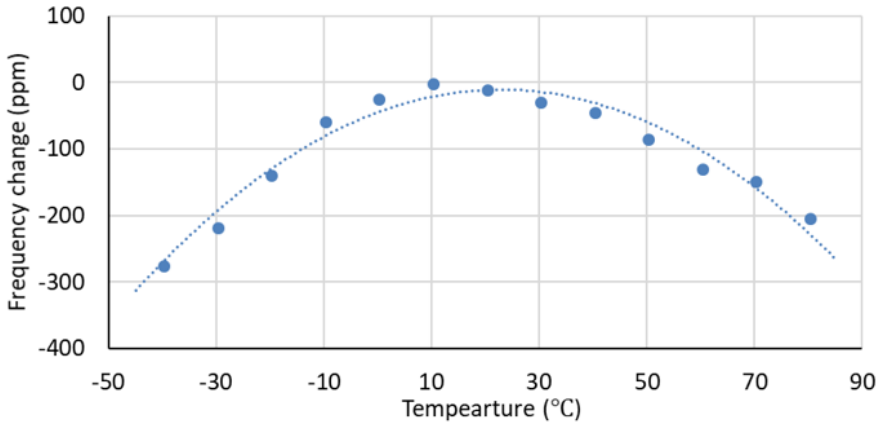

Figure 77 – Measured turnover point at 30°C for BAW accel for a doping concentration of <0.005 ohm-cm.

The acceleration testing setup of the device consisted of discrete electronics while mounted on a rate table which provides a constant acceleration of up to 20g due to centrifugal force equivalent to 2000°/s of rotation (Figure 76). This was the maximum acceleration that could be applied (20g) due to testing setup limitations. The devices were tested in a differential configuration to eliminate 1st order temperature effects and a beat frequency was extracted using a frequency counter. The chamber temperature was kept constant at 40°C. A linear scale factor of 0.91Hz/g is measured for an applied tuning voltage of 12V, for up to the 20g of acceleration range (Figure 78). Each scale factor data point was obtained by averaging a 5-minute measurement. However, there were some challenges involved in the measurement of the scale factor, which made it difficult to accurately measure the points. The temperature variation due to environmental drift and air turbulence, was comparable to the scale factor at small accelerations. These variations can be negated by on-chip temperature ovenization. It is important to note that the measured bandwidth for the device was 360kHz, defined by its translational mode frequency, which is significantly larger than conventional quasi-static accelerometers.

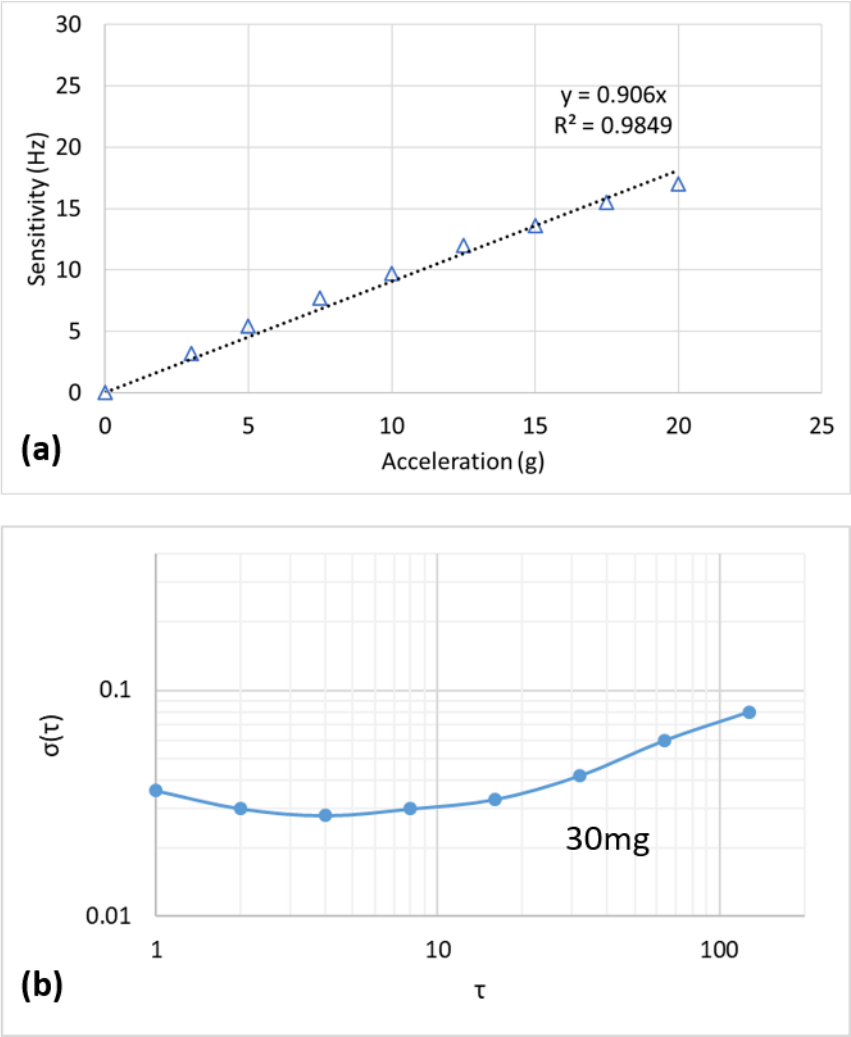

Figure 78 – Measured scale factor of 0.91Hz/g (a) and measured ADEV with a floor of 30mg (6ppb) (b).

Owing to the large doping in the silicon substrate <0.005 ohm-cm N/As, a frequency turnover point was seen with respect to temperature. This turnover point at about 30°C, allows us to ovenize the device by maintaining the temperature of the device at that temperature where the TCF is zero (Figure 77). This would help eliminate temperature drifts in the system while testing for low accelerations, where such a drift would be comparable to the frequency change due to acceleration.

CHAPTER 6. CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

This dissertation covered unique and novel designs of the three main types of inertial sensors that are used in IMUs – gyroscopes, accelerometers and timing resonators, primarily with regards to innovations in fabrication processes to achieve higher performance and also compatibility with new materials. A plethora of recipes were invented, which were not part of the earlier existing processes, which helped enable these innovations. While the results obtained in this work show appropriate working of the prototypes, these processes can be fabricated at better foundries for higher yield and also commercialization. The most notable contributions of this work are listed as follows:

- Designed a high quality factor N=3 disk gyroscope in isotropic substrate such as epipolysilicon and developed a fabrication process that is compatible with such a substrate. This helped enable high performance disk gyroscopes with ultra-high *Q*s exceeding 1M, with an ARW of 0.01deg/rthr, and showed for the first time a mode-matched gyroscope with ultra-high quality factors.
- Designed a high quality factor N=2 disk gyroscope in epipoly, capable of achieving a high *Q* of 1M across fabrication variations and ultra-low isolation of 99dB.
- Designed a novel resonator design known as the distributed lame mode resonator, which took a known concept of the lame mode and extended it to a MEMS timing element which is suitable for high frequency applications without compromising on the integration and compatibility with industry processes. This design is under a

pending US patent “U.S. Patent Application No. 16/249,749 ‘Distributed-Mode Beam and Frame Resonators for High Frequency Timing Circuits’, January 16, 2019, (GTRC ref no: 7780)”.

- Developed a cutting-edge fabrication process for combining piezoelectric and capacitive transduction using a metal-less process. This process could enable high frequency resonant accelerometers, using both piezo and capacitive methods of transduction for the same device.
- Developed a novel “moving electrode” structure, which can improve the dynamic range of the accelerometer, making it suitable for a wide range of robust, high-sensitivity applications.
- Developed new processing recipes for the above advanced processes in terms of dry etching (SCS, epipoly, AlN) and low temperature stress-free depositions (LPCVD polysilicon, TEOS, PECVD oxide).

6.2 Future Work

While a lot of the above designs for cutting-edge MEMS inertial sensors showed appreciable results in terms of fabrication and performance, a lot of future work still remains to truly take these devices to low-cost and high-yield commercialization. Considering the limitations of the University cleanroom, the standards of which not being the same as those in industry, achieving ultra-high performance from these devices in terms of bias instability was fairly restricted.

While a good performance as per design was achieved on the epipoly gyroscopes, the bias levels can still be made lower than current measurements. In order to do this, there

needs to be made available vacuum packaging techniques for these devices which will make them less susceptible to vibrations from vacuum pumps and large test setups. For this purpose, a vacuum packaged process must be developed. The bias can also be made stable with the help of better circuitry, one example of which would be to include automatic quadrature control in the feedback loop, which would prevent the quadrature from drifting. Also, while the epipoly substrate was able to prove many advantages over SCS in terms of *Q*, SF and ARW, the large mode splits were a major obstacle in achieving low bias. The likely cause of this would be the granular structure of the epipoly substrates which contain free volume between twin grains, thereby adding some residual stress in the film.

Hydrogen annealing of sidewalls of trenches etched using DRIE becomes a vital step for sub-100nm gaps. A major hindrance in the current HARPSS process flow is the sidewall scalloping and large footing at the bottom of the trenches caused by Bosch DRIE, which leads to a roughening of the sidewalls at that region. This happens due to excessive accumulation of ions at the bottom of the trench. For gap sizes of about 300nm, this might not pose as a critical issue, since there is a possibility of it being smoothened out during the oxidation. However, for smaller gaps of 100nm, the oxidation is not large enough to mitigate this, and it can be detrimental to the working of the capacitive gaps which will lead to shorting between electrodes and the device. Hence, it is imperative that these sidewalls must be smoothened out for gap sizes that are below 200nm wide.

APPENDIX A. MATLAB CODE FOR CALCULATION OF TURNOVER POINTS IN SCS BAW RESONATORS

As mentioned in section 4.2.2, the turnover points were calculated using the equations for the change of elastic constants with respect to doping concentrations at different temperatures. The code allows you to enter the doping concentration for n-doped SCS substrate in m^{-3} and outputs the TCF turnover points for those values. The MATLAB code is as follows:

A.1 TCF calculation code

```
clc;
clear all;

%% fit temperatures
t1 = 233;
t2 = 493;
for i = t1:1:t2
    m(i-t1+1,1) = i;
end

%% fit eta
m(:,2) = 25e-3./(8.6173324e-5.*m(:,1));

%% fit fermi integrals -0.5 and 0.5 resp
m(:,3) = fermi(-0.5,m(:,2));
m(:,4) = fermi(0.5,m(:,2));

%% calculating dCs for doping
% for N = 5e25:0.5e25:7e25
N = 5e25;
dC11 = -(2/9)*(9.6)^2*N*1.602176e-
19*0.5.*m(:,3)./(8.6173324e-5.*m(:,1).*m(:,4));
dC12 = (1/9)*(9.6)^2*N*1.602176e-
19*0.5.*m(:,3)./(8.6173324e-5.*m(:,1).*m(:,4));
dC44 = 0;

%% elasticity temperature coefficients
```

```
a11 = -74.87e-6;
a12 = -99.46e-6;
a44 = -57.98e-6;

%% solve for cij pure Si
% linear eq constants
A11 = 165.64e9/exp(a11*298);
A12 = 63.94e9/exp(a12*298);
A44 = 79.51e9/exp(a44*298);

c11 = A11.*exp(a11.*m(:,1));
c12 = A12.*exp(a12.*m(:,1));
c44 = A44.*exp(a44.*m(:,1));

%% calculate total change
C11 = c11 + dC11;
C12 = c12 + dC12;
C44 = c44 + dC44;

% normalized values
% nC(:,1) = ((C11-max(C11))./max(C11))*1e6;
% nC(:,2) = ((C12-max(C12))./max(C12))*1e6;
% nC(:,3) = ((C44-max(C44))./max(C44))*1e6;
%
% nc(:,1) = ((c11-max(c11))./max(c11))*1e6;
% nc(:,2) = ((c12-max(c12))./max(c12))*1e6;
% nc(:,3) = ((c44-max(c44))./max(c44))*1e6;

%% calculate E
E100 = C11 - (2.*(C12.^2)./(C11+C12));
E110 = 4.*C44.*(C11.^2 +(C11.*C12)-
(2.*(C12.^2)))./(2.*C44.*C11 + (C11.^2) + (C11.*C12) -
(2.*(C12.^2)));
Esquare = C11 + C12 - (2.*(C12.^2)./C11);
Elame = 0.5.*(C11 - C12);
t=32*pi/180;
E16 = (0.5.*(C11 - C12)).*((sin(2*t))^2) +
C44.*((cos(2*t))^2);

E100a = c11 - (2.*(c12.^2)./(c11+c12));
E110a = 4.*c44.*(c11.^2 +(c11.*c12)-
(2.*(c12.^2)))./(2.*c44.*c11 + (c11.^2) + (c11.*c12) -
(2.*(c12.^2)));
% Esquarea = C11 + C12 - (2.*(C12.^2)./C11);
Elamea = 0.5.*(c11 - c12);

n(:,1)=((E16-max(E16))/max(E16))*1e6;
```

```
%% frequency
f100 = (1/(2*120e-6)).*sqrt(E100/2330);
f110 = (1/(2*80e-6)).*sqrt(E110/2330);
flame = (1/(sqrt(2)*2030e-6)).*sqrt(Elame/(2330*2));
fsquare = (1/(sqrt(2)*2030e-6)).*sqrt(Esquare/(2330*2));
plot(m(:,1)-273,(flame-max(flame))/max(flame));grid on;hold
on;
```

A.2 Fermi function code

```
function xx=fermi(aj,eta)

%Program begins
 format long e;
% Evaluation of Trapezoidal sum begins
range=8.;
% eta = 1; aj=0.5;
if eta > 0
   range=sqrt(eta+64.);end;
h=0.5;
nmax=range/h;
% sum=[29,1];
sum=0.;
if aj== (-0.5)
   sum=1./(1.+exp(-eta));
else
   for nn=1:1:size(eta,1)
       sum(nn,1)=0;
   end;
end;
for i=1:nmax
   u=i*h;
%    for r = 1:1:29
A=2*(u.^((2*aj)+1));
B=(1+exp(u*u-eta));
% C=A/B;
   ff(:,1)=A./B(:,1);
%     ff(:,1)=ff(29,1);
%    end
   sum(:,1)=ff(:,1)+sum(:,1);end;
disp(sum);
%Trapezoidal Summation ends

% Pole correction for trapezoidal sum begins
pol=0.;
npole=0;
```

```
% Fix the starting value of BK1 to start while loop
bk1=0;
while bk1 <= 14*pi
   npole=npole+1;
   bk=(2*npole -1)*pi;
   rho=sqrt(eta.*eta+bk.*bk);
   t1=1;
   t2=0;
   if eta < 0;
      tk(:,1)=- aj.*(atan(-bk./eta)+pi);
   elseif eta ==0;
      tk(:,1)=0.5*pi.*aj;
   else
      eta > 0;
      tk(:,1)=aj.*atan(bk./eta);
   end;
   rk=- (rho.^aj);
   tk(:,1)=tk(:,1)+0.5*atan(t2/t1);
   if eta < 0
      rk= -rk;
   end;
   ak=(2.*pi/h)*sqrt(0.5*(rho+eta));
   bk1=(2.*pi/h)*sqrt(0.5*(rho-eta));
   if bk1 <= (14*pi)
   gama=exp(bk1);
   t1=gama.*sin(ak+tk)-sin(tk);
   t2=1.-2.*gama.*cos(ak)+gama.*gama;
   pol=pol+4.*pi.*rk.*t1./t2;
   end; %ends if loop above
  end; % Top while loop ends
  npole=npole-1;
  fdp=sum*h+pol;

% Program ends with the following output
  disp('Fermi-Dirac Integral Value');
  disp(fdp/gamma(1+aj));
  xx(:,1)=fdp/gamma(1+aj);
```

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